



Summary

Retargeting XC7200/XC7300 designs to the XC9500 CPLD family can be as simple as changing the device type in the Design Manager and refitting the design. The uniform architecture of the XC9500 simplifies design translation. This document assumes a version 4.2 or later Xilinx design file for the original XC7200/XC7300 format. Xilinx M1 design software translation to the XC9500 is also assumed.

1. Take the existing **.pld** file that was targeted for the XC7200/XC7300 and copy it to a new directory.
2. Invoke the Design Manager with the design file. Choose an XC9500 device to implement the design. Automatic part selection may be appropriate.

Xilinx Family

XC7200, XC7300, and XC9500.

Technical Issues when Converting Designs from XC7200/XC7300 to XC9500

Ideally, taking an XC7200/XC7300 design file and targeting to an XC9500 device is as simple as changing the device type in the Design Manager. Because there are differences between the two family architectures, there are a few technical issues that the designer should be aware of when making the transition. Also, the pinouts differ.

1. XC9500 JTAG Pins Unusable for I/O.

XC7200/XC7300 I/O pins occupying the XC9500 JTAG pins must be moved to other sites. If there are not enough pins, the design must be fit into a larger package. If no larger packages exist, then move to the next larger device and package with more I/O pins. Refer to the data sheet for specific pins for your part and package.

2. XC9500 Family does not Support Hardware Arithmetic

Designs using the XC7200/XC7300 arithmetic functions must be manually retargeted to the XC9500 family. This involves insertion of equivalent gate substitutions for arithmetic macrocell configurations. Note that since there are no special arithmetic paths and logic, the design may take a slightly larger part to implement the original design. Manual intervention with the **.pld** file will be required. Contact Xilinx Factory Technical Support for assistance.

3. The Functions Blocks are Different

If you have constrained your XC7200/XC7300 design to certain function blocks and macrocells, your new design may have problems fitting. Remember, there are more macrocells per function block in an XC9500, as well as fewer function blocks. Old constraints may be invalid in some cases. Releasing design constraints allows the fitter to move logic around to best fit your design.

4. Input Registers Map to Macrocells

Designs using input registers will use more macrocells to replace the XC7200/XC7300 input registers. A larger number of macrocells may be required on the new XC9500 design. Timing must be checked for design compatibility. This may be solved by using faster XC9500 parts.

5. There is no Master-Reset Signal

If an XC7200/XC7300 MR pin is being driven by a global reset in the system, the design must be recompiled to use the GSR pin available on XC9500 parts.

Table 1 summarizes target XC9500 options.

Table 1: XC7200/XC7300 to XC9500 Devices

Old Device	New Device	Possible Issues
XC7236A	XC9536 XC9572	1, 3, 5
XC7272A	XC9572 XC95108	1, 2, 3, 4, 5
XC7336	XC9536 XC9572	1, 3, 5
XC7354*	XC9572	1, 2, 3, 4, 5
XC7372	XC9572 XC95108	1, 2, 3, 4, 5
XC73108	XC95108 XC95216	1, 2, 3, 4, 5
XC73144	XC95216	1, 2, 3, 4, 5

*This upgrade will require a package change..

By converting now to the XC9500 family, you can gain the advantages of speed, power, improved fitting, and, of course, in-system programming.



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