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VERY LARGE TELESCOPE

TIME REFERENCE SYSTEM, TIME INTERFACE MODULE, TECHNICAL MANUAL

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CHANGE RECORD.

Issue:	Date:	Section/Page affected:	Comments:
1	18 Aug. 1993	All	First issue, replacing previous drafts.
draft for iss. 2	23 Jun. 1994	All	Complete new issue, for changes see VLT-ELE-94/0072.
2nd draft for iss. 2	21 Dec. 1994	Cover page Ch. 1.2.3 Ch. 1.2.5 Ch. 2.1. Ch. 2.2. 2.3 5.2.3.5	Indicate new draft. Ref to Micro Crystal removed. Power req'd from 12V updated. Default jumper settings updated. Reference to special card added. P3 pin assignment updated. Note 1 removed.
3rd draft for iss. 2	6 Feb. 1995	Ch. 2.1	Plots for jumper settings added.
4th draft for iss. 2	21 Feb. 1995	Ch. 2.1.6 Ch. 6.4	New chapter. Loading timing made more clear.
2	11 Jul. 1995	Ch. 1.3 Ch. 2.1.3 Ch. 2.1.3 Ch. 2.1.6	New chapter. Reference to ch. 1.3 added. Default IRQ level changed from 4 to 7 Description made more clear.

TABLE OF CONTENTS

1. GENERAL INFORMATION

1.1. INTRODUCTION

The Time Interface Module (TIM) is the VME module in the Local Control Units that need accurate Universal Time Coordinated (UTC) for the purpose of synchronisation and/or tracking.

This manual uses the notation '0x....' or '.... hex' to indicate hexadecimal numbers.

1.2. SPECIFICATIONS

1.2.1. FUNCTIONS

The TIM provides the following functions:

a. reception and decoding of the serialised UTC signal from the Time Bus.
b. back-up frequency standard.
c. UTC counter and register, accessible from the VME bus.
d. Cyclic interrupts from this register, one interrupt every 10 ms and one every 1 second.
e. 6 programmable general purpose timers, each 16 bit.

Function a. through d. form the 'UTC section', while function e. forms the 'Timer section' of the TIM.

1.2.2. PROPAGATION DELAY

Propagation delay from (Fiber Optic) Time Bus input to:	
the VME interrupt request (IRQx):	< 350 nanosec (typ. 300 ns)
the significant edge of the timer output on P2:	< 250 nanosec (typ. 200 ns)
the significant edge of the frequency outputs on P2:	< 250 nanosec (typ. 200 ns)

1.2.3. LOCAL MODE

Error in the time at a switching from 'normal' to 'local' mode:	< 2 microsec (typ. 1.5 microsec)
Overall frequency stability of the quartz oscillator:	< +/- 100 ppm

1.2.4. VME BUS CONNECTION

Compliant with VME bus specification ANSI/IEEE Std 1014-1987, with the options set as:

Type:	slave module
Mechanical:	double height
Address:	A16, board occupies 128 bytes of memory space. ADO (tolerates Address Only cycles)
Address modifier:	29 hex or 2D hex (short supervisory and short non privileged I/O)
Data:	D16, D08(EO).
Interrupter:.	D08(O), I(1-7), RORA

1.2.5. POWER REQUIREMENTS

650 mA typ. @ 5V
0 mA @ -12V

The current consumption from the +12V supply depends on the hardware option which is selected for the Time Bus connection:

Time Bus:	Current from +12V:
front	0 mA
P2, JP5 out	20 mA typ.
P2, JP5 in	40 mA typ.

1.2.6. INDICATORS

Three LEDS are mounted on the front panel as status indicators:

Indicator:	Color:	Meaning:
TBOK	green	If on, the TBOK signal is detected.
1Hz	yellow	Flashes with a frequency of 1Hz.
LOCAL	red	If on, the TIM is in local mode.

1.3. BOARD REVISIONS

This document describes board revision 1.
Some boards with serial number less than 10 have revision 0, which has been upgraded by artwork into rev. 1. The assignment of jumper area JP3 (IRQ level) is however different than the one of rev. 1. This is clearly indicated with a label, glued on U14. Apart from that, upgraded rev. 0 boards are fully compliant with this document.

2. PREPARATION FOR USE

This chapter describes the actions that are necessary before the TIM can be used in a VME system.

2.1. JUMPER SETTINGS

2.1.1. JUMPER LOCATIONS

Fig. 1 shows the overall layout of the Printed Circuit Board with the jumper locations.

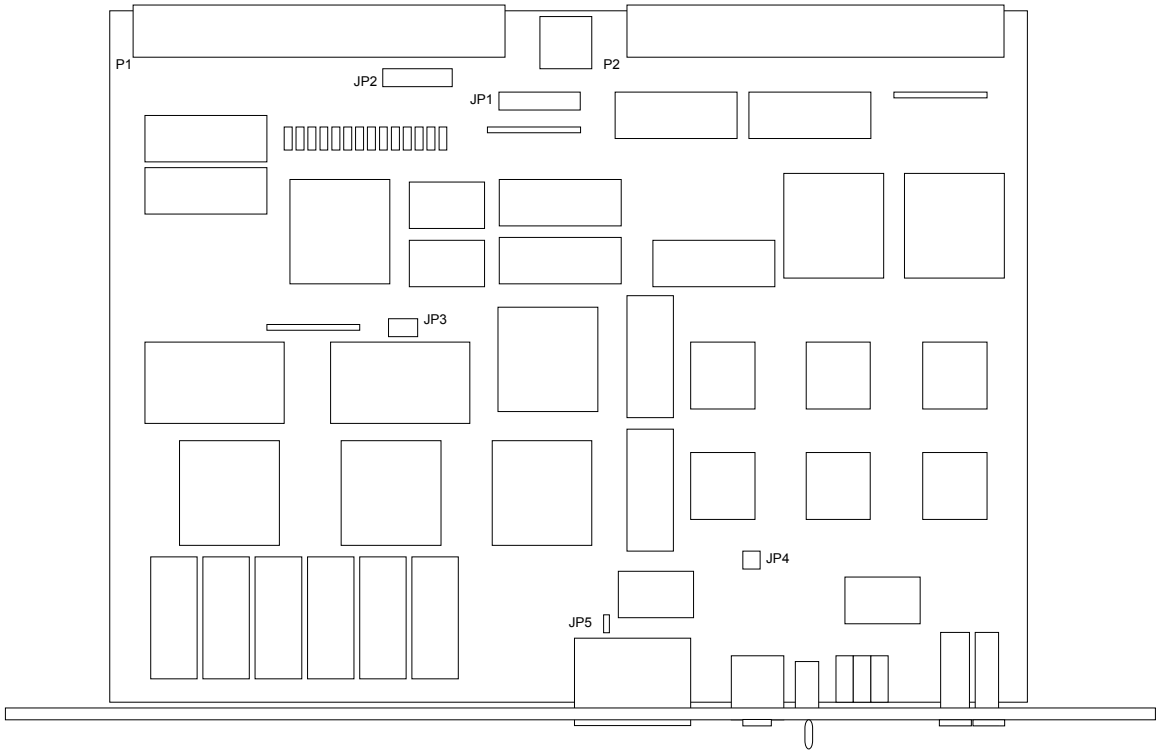


Fig. 1. Jumper locations.

2.1.2. BOARD BASE ADDRESS

The board base address is set by JP1 and allows setting on any 128 byte boundary of the Short I/O VME address space.
Each jumper controls an address bit. The jumper must be placed to make the address bit '1' and must be removed to make the address bit '0'.

JP1 jumper:	Base address: (hex)
1-2 in	8000
3-4 in	4000
5-6 in	2000
7-8 in	1000
9-10 in	800
11-12 in	400
13-14 in	200
15-16 in	100
17-18 in	80

Default setting: Address 100 hex.
The location and the pin numbering of JP1 is shown in fig. 2.

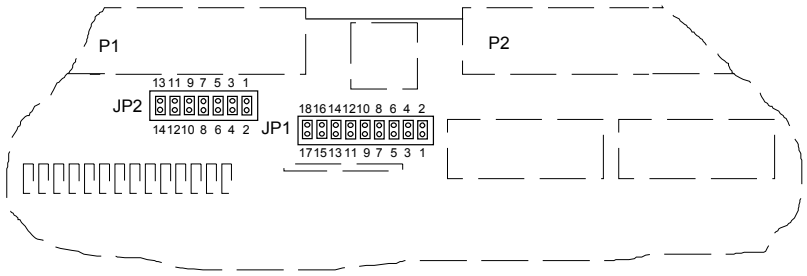


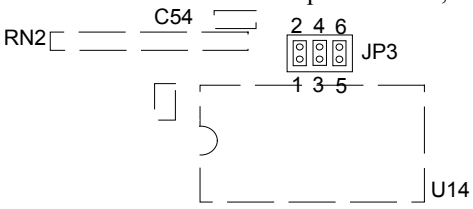
Fig.2. JP1 and JP2 jumper pin numbering.

2.1.3. VME INTERRUPT REQUEST LEVEL

The interrupt request level is set by JP2 and JP3.
JP2 controls the assignment to the VME IRQ lines while JP3 controls the decoding of the VME address lines 1 through 3.
JP2 and JP3 must be set such that they correspond with the same VME IRQ level:

JP2 jumper:	JP3 jumper:	VME IRQ level:
1-2 in	1-2 in	IRQ 1 (lowest priority)
3-4 in	3-4 in	IRQ 2
5-6 in	1-2 and 3-4 in	IRQ 3
7-8 in	5-6 in	IRQ 4
9-10 in	5-6 and 1-2 in	IRQ 5
11-12 in	5-6 and 3-4 in	IRQ 6
13-14 in	5-6 and 1-2 and 3-4 in	IRQ 7 (highest priority)

Default setting: IRQ level 7.
The location and the pin numbering of JP2 is shown in fig. 2. The location and the pin numbering of JP3 is shown in fig. 3.
Note: printed circuits boards with rev. 0 have a different footprint for JP3, see chapter 1.3.



TOP VIEW

Fig. 3. JP3 jumper pin numbering.

2.1.4. TIME BUS SIGNAL SOURCE.

The Time Bus signal source is selected with JP4:

JP4 jumper:	Time Bus signal source:
1-2 in	Via the P2 connector (RS485 logic levels)
3-4 in	Via the front panel fiber optic connector

Default setting: Time Bus signal via P2.
The location and the pin numbering of JP4 is shown in fig. 4.

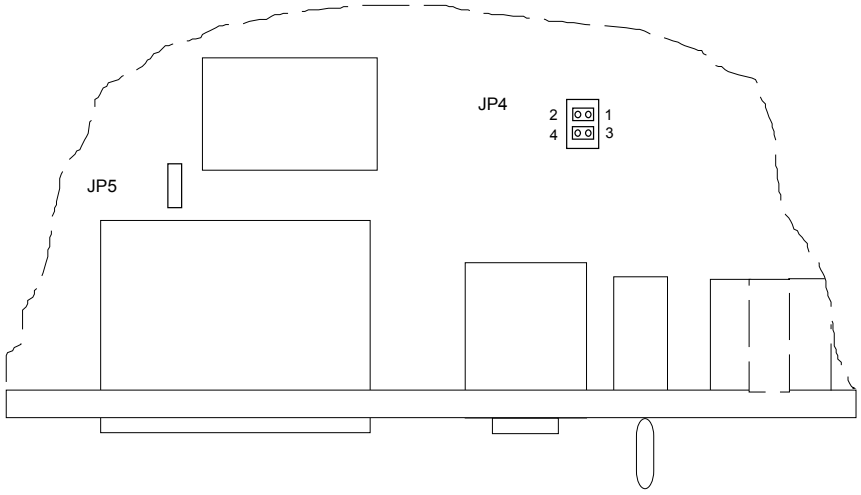


Fig. 4. JP4 and JP5 jumper pin numbering.

2.1.5. TIME BUS SIGNAL TERMINATION

If the Time Bus signal is entered via P2 (as can be selected with JP4, see chapter 2.1.4.), the signal can be terminated with a 120 Ohm resistor. This is necessary if the cable between P2 and the (Fiber Optic) Time Bus receiver is longer than 3 meters. The termination is controlled with JP5:

JP5 jumper:	Termination:
1-2 out	No termination.
1-2 in	120 Ohm termination.

Default setting: No termination.
The location and the pin numbering of JP5 is shown in fig. 4.

2.1.6. BACKPLANE RECEIVER

The Time Bus should enter via P2 in a typical installation. This avoids the need to connect the (fragile) fiber via the front panel. A small printed circuit board, which receives the optical Time Bus signal and transforms it into a differential TTL signal, is available for that purpose. This PCB is identified as 'TIM Backplane Receiver'. It must be mounted in the VME chassis such that the P2 connector of the TIM board fits into the J1 connector of the Backplane Receiver.
All TIM P2 connections (as listed in chapter 2.2.), except the Time Bus + and Time Bus - signals, are available on the J2 connector of the TIM Backplane Receiver with the same pin assignment.
The JP1 on the TIM Backplane Receiver allows the following selection for the Time Bus signal:

JP1 jumper (on Backplane Receiver):	Time Bus Connection (U3 is the fiber optical connector on the Backplane Receiver):
1-2 in, 5-6 in:	Time Bus fiber connected on TIM backplane receiver (U3), route to TIM P2 *only*. (Default setting)
1-2, 3-4, 5-6, 7-8 (all 4 jumpers in):	Time Bus fiber connected on TIM backplane receiver (U3), route to TIM P2 *and* Backplane Receiver J2.
3-4 in, 7-8 in:	Receive Time Bus from Backplane Receiver J2; i.e. do not use the fiber optical receiver on the TIM backplane receiver (U3).
Other combinations:	illegal.

The location and the pin numbering of JP1 on the TIM Backplane Receiver are shown in fig. 5.

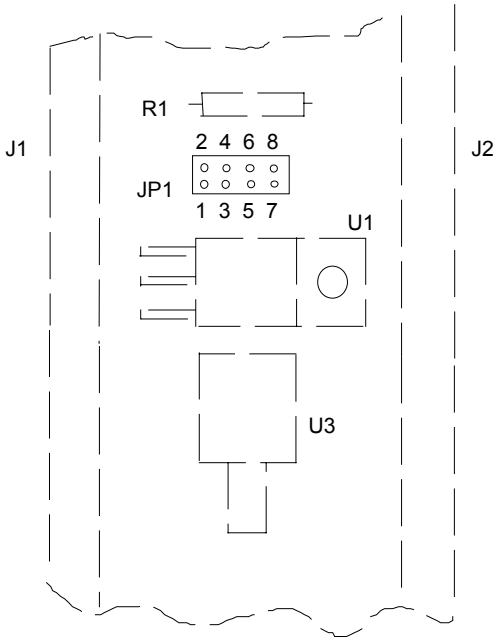


Fig. 5. TIM Backplane Receiver JP1 jumper pin numbering.

2.2. P2 CONNECTIONS

The P2 connector allows interfacing of the TIM to user specific hardware. There is also the possibility to enter the Time Bus signal via P2 as a symmetrical logic (RS485 logic levels).
The special card, indicated as TIMP2, is available to connect the (fiber optic) Time Bus via the P2 connector.

All outputs are driven by a HCT541 type driver which drives the corresponding P2 pin only. Inputs are fed to CMOS gates with TTL compatible levels.

The frequency outputs are described in detail in chapter 4.1.1.

P2 pin:	Function:	P2 pin:	Function:
A1	Frequency output 7	C1	Dig. ground
A2	Frequency output 6	C2	Dig. ground
A3	Frequency output 5	C3	Dig. ground
A4	Frequency output 4	C4	Dig. ground
A5	Frequency output 3	C5	Dig. ground
A6	Frequency output 2	C6	Dig. ground
A7	Frequency output 1	C7	Dig. ground
A8	Frequency output 0	C8	Dig. ground
A9	Timer 5 output	C9	Dig. ground
A10	Timer 4 output	C10	Dig. ground
A11	Timer 3 output	C11	Dig. ground
A12	Timer 2 output	C12	Dig. ground
A13	Timer 1 output	C13	Dig. ground
A14	Timer 0 output	C14	Dig. ground
A15	Testpoint (Interrupt to VME bus)	C15	Dig. ground
A16	Spare output, set to low TTL level	C16	Dig. ground

A17	Timer 5 gate input	C17	Dig. ground
A18	Timer 4 gate input	C18	Dig. ground
A19	Timer 3 gate input	C19	Dig. ground
A20	Timer 2 gate input	C20	Dig. ground
A21	Timer 1 gate input	C21	Dig. ground
A22	Timer 0 gate input	C22	Dig. ground
A23	Dig. ground	C23	Dig. ground
A24	Time Bus + (RS485) input	C24	Dig. ground
A25	Time Bus - (RS485) input	C25	Dig. ground
A26	Dig. ground	C26	Dig. ground
A27	Not connected	C27	Dig. ground
A28	Not connected	C28	Dig. ground
A29	Not connected	C29	Dig. ground
A30	Not connected	C30	Dig. ground
A31	VME -12 Volt	C31	VME +12 Volt
A32	VME +5 Volt	C32	VME + 5 Volt

2.3. DISPLAY CONNECTIONS

The signal that is received from the Time Bus is available as an open collector TTL signal on the Display connector (P3) on the front panel. A 5V with a 270 Ohms series resistor is also available. There is no power for the display available: the input of the display must be a diode of an optocoupler.

P3 pin:	Function:
1	Dig. ground
2	Not connected
3	Not connected
4	Time Bus signal (open coll. TTL)
5	Connected to pin 9
6	Dig. ground
7	Not connected
8	Not connected
9	Pull-up (270 Ohms) to +5V

3. MEMORY MAP

The TIM board occupies 128 (decimal) bytes of memory address space. The base address is jumper programmable as described in chapter 2.1.

The 'high byte' is defined as data bit 15 through 8, while the 'low byte' is bit 7 through 0.

Bit 15 (or bit 7) is the most significant bit.

Base+ (hex)	High byte (D15 through D8)	Low byte (D7 through D0)
0	timer 0 config	timer 0 data
2	timer 1 config	timer 1 data
4	timer 2 config	timer 2 data
6	not used	timer control, 0 through 2
8	timer 3 config	timer 3 data
a	timer 4 config	timer 4 data
c	timer 5 config	timer 5 data
e	not used	timer control, 3 through 5
10	interrupt source	interrupt status/ID
12	UTC status	UTC status
14	not used	not used
16	not used	not used
18	0	microsec, high byte
1a	microsec, middle byte	microsec, low byte
1c	minutes	seconds
1e	not used	hours
20	0	Modif. Julian Day, high byte
22	Modif. Julian Day, middle byte	Modif. Julian Day, low byte
24	and upwards: not used	

Note: 'not used' results in a reading of 0xff.

4. PROGRAMMING INFORMATION, TIMER SECTION

4.1. GENERAL

The programmable timers are based upon the 82C54 timer chip, which contains 3 timers.
There is one timer control register per three timers. There are 2 chips implemented, resulting in a total of 6 timers. The 6 timers are numbered: 0 through 5.

Each timer has an associated configuration register, where the clock frequency, gating and interrupt can be programmed.

The timer functions are selected by writing of the CPU into the control register.

Each timer operating mode is set by (in this sequence):

- configuration register programming (select clock frequency),
- control register programming,
- data register programming,
- configuration register programming (select gating and interrupt mode).

The timers are set to 0000 hex during control register setting. The timer value 0000 hex cannot be read.

The output of each timer can generate interrupt if the interrupt is enabled.

The timer data bus is 8 bit wide. In order to use 16 bit count values, the control register has to be programmed accordingly and the 2 bytes with the count value can be loaded sequentially into the data register.

The configuration registers are not part of the timer chip. They provide:

- selection of clock frequency.
- selection of timer gating source.
- interrupt enable and interrupt clear.
- status of timer gating signal (VME read only).

4.1.1. CLOCK FREQUENCY.

The clock frequency can be programmed from 1 Hz to 1 MHz in steps of a factor 10.
The clock frequencies are synchronous with the Universal Time Coordinated, generated by the UTC section of the module.
The timers use the falling edge of the clocks as the active one.

In addition, there is the possibility to select a frequency 0 (set clock signal to low logic level). This is used during the set-up to set 'gate next 100 millisecond', see chapter 4.1.2.

4.1.2. GATING SOURCE.

The gating source can be programmed, one out of 4 possible sources:

- Clear gate signal, timer stops.
- (External) hardware gating signal.
- Set gate signal, timer runs.
- Set gate signal at the next 100 millisecond.

The last mode allows synchronisation of more than one timer, even if they are in different LCU's.
However, the timer needs to be set up in the following sequence to provide proper and unambiguous start:

- After a 100 millisecond edge, the timer is first set to 'clear gate' mode with clock frequency 0 Hz (= low logic level).
- Program timer mode and count value.
- Set 'gate next 100 millisecond', clock frequency and, if needed, interrupt enable.

One has to make sure that this timer set-up is finished before the 'next' 100 millisecond comes. Only in that case one can be sure of the correct start of the timer.

Notes:

1. The timer is loaded at the edge of the 'next' 100 millisecond. There is no timer output pulse at that moment. From that moment on, clock pulses are fed to the timer.
2. If a repetitive mode is selected: the time between the '100 millisecond edge' to the first rising timer output is the same as between the first and the second rising edge of the timer output.

4.1.3. INTERRUPT

Each timer can be enabled to generate an interrupt signal to the VME bus. The rising edge of the timer output sets its interrupt flip flop.

Each interrupt has to be cleared by setting and clearing the Interrupt Clear bit, which clears the interrupt flip flop. This has to be done by the interrupt service routine (Release On Register Access, RORA).

4.2. TIMER PROGRAMMING

4.2.1. TIMER MODES

Note: the maximum count value in all modes is 0, this executes a count of 10000 hex.
The minimal count is 1 or 2, dependent on the mode.

Mode 0, Event counter.

Output operation:

The output is set to 'L' level by the control register setting, and kept at 'L' level until the timer value becomes 0.

Gate function:

A 'H' level validates the count operation, and 'L' level invalidates it. The gate does not affect the count. If the gate is set to 'L' while the output is 'H', the output will change to 'L' (see below).

Count value timing:

After the control register and the initial count value are written, the count value is loaded to the timer at the falling edge of the next clock pulse. The first clock pulse does not cause the count value to be decremented. In other words, if the initial count is set to N, the output is not set to 'H' until the input of (N+1) clock pulses after the initial count value writing.

Count value writing during counting:

The count value is loaded in the timer at the falling edge of the next clock, and the counting with the new count value continues. The operation for two byte counting is:

- The counting operation is suspended when the first byte is written. The output is immediately set to 'L' level; no clock pulse is required.
- After the second byte is written, the new count value is loaded to the timer at the falling edge of the next clock. For the output to go to 'H' level again, N+1 clock pulses are necessary after the new count value N is written.

Count value writing:

When the gate signal is 'L' level: the count value is also loaded to the timer at the falling edge of the next clock pulse in this case. When the gate signal is set to 'H' level, the output is set to 'H' level after the lapse of N clock pulses. Since the count value is already loaded in the timer, no clock pulse for performing this is necessary.

Minimum count value: 1.

Mode 1, Digital One Shot

Output operation:

The output is set to 'H' level by the control register setting. It is set to 'L' level at the falling edge of the clock succeeding the gate trigger, and kept at 'L' level until the timer value becomes 0. Once the output is set to 'H' level, it is kept at 'H' level until the clock pulse succeeding the next trigger pulse.

Count value load timing:

After the control register and initial count are written, the count value is loaded to the timer at the falling edge of the clock pulse succeeding the gate trigger and set the output to 'L' level. The one shot pulse starts in this way. If the initial count value is N, the one shot pulse interval equals N clock pulses. The one shot pulse is not repetitive.

Gate function:

The gate signal setting to 'L' level after the gate trigger does not affect the output. When it is set to 'H' level again from 'L' level, gate retriggering occurs, the timer value is loaded again and counting continues.

Count value writing during counting:

It does not affect the one shot pulse being counted until retriggering occurs.

Minimum count value: 1

Mode 2, Rate generator.

Output operation:

The output is set to 'H' level by the control register setting. When the initial count value is decremented to 1, the output is set to 'L' level during one clock pulse, and then set to 'H' level again. The initial count value is reloaded, and the above sequence repeats. In mode 2, the same sequence is repeated at intervals of N clock pulses it the initial count value is N for example.

Gate function:

'H' level validates counting and 'L' level invalidates it. If the gate signal is set to 'L' level when the output pulse is at 'L' level, the output is immediately set to 'H' level. At the falling edge of the clock pulse succeeding the trigger, the count value is reloaded and counting starts.

Count value load timing:

After the control register and initial count value is written, the count value is loaded into the timer at the falling edge of the next clock pulse. The output is set to 'L' level upon the lapse of N clock pulses after writing the initial count value N.

Count value writing during counting:

Count value does not affect the current counting operation sequence. If new count value writing completes and the gate trigger arrives before the end of current counting operation, the count value is loaded into the timer at the falling edge of the next clock pulse and counting continues from the new count value. If no gate trigger arrives, the new count value is loaded to the timer at the end of the current counting operation cycle. In mode 2, count value of 1 is prohibited.

Minimum count value: 2.

Mode 3, Square wave generator.

Output operation:

Same as mode 2, except that the output duty is different.

The output is set to 'H' level by control register setting. When the count becomes half the initial count value, the output is set to 'L' level and kept at 'L' level during the remainder of the count.

Gate operation:

A 'H' level validates counting, and 'L' level invalidates it. If the gate signal is set to 'L' level then the output is at 'L' level, the output is immediately set to 'H' level.

The initial count value is reloaded at the falling edge of the clock pulse succeeding the next gate trigger. The gate pulse can be used for timer synchronisation in this way.

Count value load timing:

After the control register and initial count value are written, the count value is loaded into the timer at the falling edge of the next clock pulse. Timer synchronisation by software is possible in this way.

Count value writing during counting:

The count value writing does not affect the current counting operation. When the gate trigger input arrives before the end of a half cycle of the square wave after writing the new count value, the new count value is loaded into the timer at the falling edge of the next clock pulse and counting continues using the new count value. If there is no gate trigger, the new count value is loaded at the end of the half cycle and counting continues.

Even number counting operation:

The output is initially set to 'H' level. The initial count value is loaded to the timer at the falling edge of the next clock pulse, and is decremented by 2 by consecutive clock pulses. When the timer value becomes 2, the output is set to 'L' level, the initial value is reloaded and then the above operation is repeated.

Odd number counting operation:

The output is initially set to 'H' level. At the falling edge of the next clock pulse, the initial count value minus one is loaded in the timer, and then the value is decremented by 2 by consecutive clock pulses. When the timer becomes 0, the output is set to 'L' level, and then the initial count value minus one is reloaded to the timer. The value is then decremented by 2 by consecutive clock pulses. When the timer value becomes 2, the output is again set to 'H' level and the initial count value minus 1 is again reloaded. The above operations are repeated. In other words, the output is set to 'H' level during (N+1)/2 counting and to 'L' level during (N-1)/2 counting in the case of odd number counting.

Minimum count value: 2.

Mode 4, Software triggered strobe.

Output operation:

The output is initially set to 'H' level. When the timer value becomes 0, the output goes to 'L' level during one clock pulse, and then restores 'H' level again.

The counting sequence starts when the initial count value is written.

Gate function:

A 'H' level validates counting, and 'L' level invalidates counting. The gate signal does not affect the count.

Count value load timing:

After the control register and initial count values are written, the count value is loaded to the timer at the falling edge of the clock pulse. The clock pulse does not decrement the initial count value. If the initial count value is N, the strobe is not output unless N+1 clock pulses are input after the initial count value is written.

Count value writing during counting:

The new count value is written to the timer at the falling edge of the next clock pulse, and counting continues using the new count value.

The operation for 2 byte count is as follows:

- First byte writing does not affect the counting operation.
- After the second byte is written, the new count value is loaded to the timer at the falling edge of the next clock pulse.

This means that the counting operation is retriggered by software. The output strobe is set to 'L' level upon input of N+1 clock pulses after the new count value is written.

Minimum count value: 1.

Mode 5, Hardware triggered strobe.

Output operation:

The output is initially set to 'H' level. When the timer value becomes 0 after triggering by the rising edge of the gate pulse, the output goes to 'L' level during one clock pulse, and then restores 'H' level.

Count value load timing:

Even after the control register and initial count values are written, loading to the timer does not occur until the input of a clock pulse succeeding the trigger. For the clock pulse for the timer loading, the count value is not decremented. If the initial count value is N, the output is not set to 'L' level until N+1 clock pulses are input after triggering.

Gate function:

The initial count is loaded to the timer at the falling edge of the clock pulse succeeding gate triggering. The count sequence can be retriggered. The gate pulse does not affect the output.

Count value writing during counting:

The count value writing does not affect the current counting sequence. If the gate trigger is generated after the new count value is written and before the current counting ends, the new count value is loaded to the timer at the falling edge of the next clock pulse, and counting continues using the new count value.

Minimum count value: 1.

4.2.2. GATING SUMMARY

Mode:	Gating: L level, falling edge:	Rising edge:	H level:
0	No counting	-	Counting
1	-	1. Start counting, 2. Retriggering	-
2	No counting, output to H level	Start counting	Counting
3	No counting, output to H level	Start counting	Counting
4	No counting	-	Counting
5	-	1. Start counting, 2. Retriggering	-

4.2.3. READING TIMER VALUES

All timers are down counting, the counting being in steps of 2 in mode 3. Timer values can be read during counting by:

- direct reading,
- timer latching, or
- read back command.

4.2.3.1. Direct reading

Timer values can be read by reading operations to the timer data register. It is necessary to stop the counting by a gate signal, as the timing between the read operation and the timer clock signal is not guarantied.

4.2.3.2. Timer latching

The timer is latched by writing a timer latch command, thereby enabling a stable value to be read without affecting the counting in any way at all. The output latch of the timer latches the count value when a timer latch command is written. The count value is held until it is read by the CPU or the control register is set again.
If a timer latch command is written again before reading while a certain timer is latched, the second timer latch command is ignored and the value latched by the first timer latch command is maintained.

When a timer is programmed for the 2 byte timer value, the following sequence is possible:

- Count value (LSB) reading.
- New count value (LSB) writing.
- Count value (MSB) reading.
- New count value (MSB) writing.

4.2.3.3. Read back command

Use of the read back command allows the user to check the count value, program mode, timer output state and null count flag of the selected timer.
The command is written in the control register.
It is possible to latch multiple timers by using the read back command. Latching of a read timer is automatically cancelled but other timers are kept latched. If multiple read back commands are written for the same timer, commands other than the first one are ignored.

It is also possible to latch the status information of each timer by using the read back command. The status of a certain timer is read when the timer data register is read.

Null count indicates that the count value finally written in the timer data register has been loaded in the timer. The time when the count value was loaded in the timer depends on the mode of each timer, and it cannot be known by reading the timer value because the count value does not tell the new count value if the timer is latched.
The null count operation is:

Operation:	Result:
Control register writing	Null count=1
Data register writing	Null count=1
New count load to timer	Null count=0

The null count operation for each timer is independent. When the 2 byte count is programmed, the null count is set to 1 when the count value of the second byte is written.

If both the count and status are latched, the status latched in the first read operation to the timer data register is read. The order of count latching and status latching is irrelevant. The count(s) of the next one or two reading operations is or are read.
If status latching is carried out multiple times before status reading, other than the first status latch is ignored.

Simultaneous latching of the count and status of the selected timer is also possible. For this purpose, set bits D4 and D3, COUNT\ and STAT\ bits, to '00'. This is functionally the same as writing two separate read back commands at the same time. If timer/status latching is carried out multiple times before reading, other than the first one is ignored here again.

4.3. TIMER REGISTER ASSIGNMENT

4.3.1. TIMER CONTROL REGISTER

Location: Base+0x6 (for timer 0 through 2) or Base+0xE (for timer 3 through 5), low byte

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	RL1	RL0	M2	M1	M0	BCD
Select timer		Read/Load		Mode			BCD

SC1	SC0	Set contents
0	0	Timer # 0 selection (# 3 respectively)
0	1	Timer # 1 selection (# 4 resp.)
1	0	Timer # 2 selection (# 5 resp.)
1	1	Read back command, see note

Note: the 'Read back command' uses different assignment for D5 through D0. See chapter 4.3.3.

RL1	RL0	Set contents
0	0	Timer latch operation
0	1	Reading/Loading of Least Significant Byte
1	0	Reading/Loading of Most Significant Byte
1	1	Reading/Loading of LSB followed by MSB

M2	M1	M0	Set contents
0	0	0	Mode 0, Interrupt on terminal count
0	0	1	Mode 1, Programmable one shot
0	1	0	Mode 2, Rate generator
x	1	1	Mode 3, Square wave generator
1	0	0	Mode 4, Software triggered strobe
1	0	1	Mode 5, Hardware triggered strobe

BCD	Set contents
0	Binary count (8 or 16 bits binary, depending on setting of RL bits)
1	BCD count (2 or 4 decades BCD, depending on setting of RL bits)

4.3.2. TIMER DATA REGISTER

The data register allows writing and reading the count values.

Locations:
Base + 0x0, low byte: timer 0,
Base + 0x2, low byte: timer 1,
Base + 0x4, low byte: timer 2,
Base + 0x8, low byte: timer 3,

Base + 0xA, low byte: timer 4,
Base + 0xC, low byte: timer 5.

D7	D6	D5	D4	D3	D2	D1	D0
MSB...							...LSB

4.3.3. CONTROL & DATA REGISTER FOR READ BACK.

4.3.3.1. Control register (write)

Location: Base+0x6 (for timer 0 through 2) or Base+0xE (for timer 3 through 5), low byte

D7	D6	D5	D4	D3	D2	D1	D0
1	1	COUNT\	STAT\	CNT2	CNT1	CNT0	0

D7, D6: '1' (Read back select).
D5: '0'= Selected timer count latch operation.
D4: '0'= Selected timer status latch operation.
D3: '1'= Timer # 2 (5 resp.) selection.
D2: '1'= Timer # 1 (4 resp.) selection.
D1: '1'= Timer # 0 (3 resp.) selection.
D0: '0'= Fixed.

4.3.3.2. Data register (read)

Locations:
Base + 0x0, low byte: timer 0,
Base + 0x2, low byte: timer 1,
Base + 0x4, low byte: timer 2,
Base + 0x8, low byte: timer 3,
Base + 0xA, low byte: timer 4,
Base + 0xC, low byte: timer 5.

D7	D6	D5	D4	D3	D2	D1	D0
OUT	NULL	RL1	RL0	M2	M1	M0	BCD

D7: '1'= Output pin status is 1.
'0'= Output pin status is 0.
D6: '1'= Null count.
'0'= Count value register is effective.
D5 through D0: Programmed mode of the timer. See chapter 4.3.1.

4.3.4. TIMER CONFIGURATION REGISTER

It is useful to write into the timer configuration register by using byte access: the configuration register is are in the same (16 bit) word as the timer data register. Writing to the data register results in a new count value.

Locations:
Base + 0x0, high byte timer 0,
Base + 0x2, high byte timer 1,
Base + 0x4, high byte timer 2,
Base + 0x8, high byte timer 3,
Base + 0xA, high byte timer 4,
Base + 0xC, high byte timer 5.

D15	D14	D13	D12	D11	D10	D9	D8
CLSEL2	CLSEL1	CLSEL0	GS1	GS0	IENAB	ICLEAR	GATE

The status after VME SYSRESET is 00 hex.

CLSEL2	CLSEL1	CLSEL0	Timer clock frequency:
0	0	0	1 Hz
0	0	1	10 Hz
0	1	0	100 Hz
0	1	1	1 kHz
1	0	0	10 kHz
1	0	1	100 kHz
1	1	0	1 MHz
1	1	1	- (0 Hz)

GS1	GS0	Gating source signal:
0	0	'0', stops counting
0	1	External hardware gate signal
1	0	'1', allows counting
1	1	Gate at active edge of next 100 millisec

IENAB	
0	Interrupt disabled
1	Interrupt enabled

ICLEAR	
0	Interrupt possible
1	Interrupt clear

GATE	
0	Timer is not gated (VME read only)
1	Timer is gated (VME read only)

4.3.5. INTERRUPT SOURCE REGISTER

This is a VME read only register.
A bit value '1' indicates a pending interrupt.

Location: Base + 0x10, high byte.

D15	D14	D13	D12	D11	D10	D9	D8
INT7	INT6	INT5	INT4	INT3	INT2	INT1	INT0

The status after VME SYSRESET is 00 hex.

INT7: UTC 10 millisec.
INT6: UTC 1 second.

INT5: timer 5
INT4: timer 4
INT3: timer 3
INT2: timer 2
INT1: timer 1
INT0: timer 0

4.3.6. INTERRUPT STATUS/ID REGISTER

This is a read / write register. Read is provided for verification and test purposes. The 8 bit status/ID is put on the VME bus during the Interrupt acknowledge cycle.

Location:
Base + 0x10, low byte.

D7	D6	D5	D4	D3	D2	D1	D0
MSB...							...LSB

The status after VME SYSRESET is UNDEFINED.

5. PROGRAMMING INFORMATION, UTC SECTION

5.1. GENERAL

The UTC is received from the Time Bus. The Time Bus signal is a serial coded UTC signal that is loaded into the UTC counter. Note that the clocking of the UTC counter is done synchronous, the loading is synchronous as well.

The UTC counter can be latched into registers by a VME 'FREEZEIN' signal. This signal is clocked with the counting clock to provide unambiguous latching. The registers can then be read from the VME side.

5.1.1. LOCAL MODE

When there is no Time Bus signal available, the TIM switches (by the hardware) to local mode, which means:

- the TIM uses an on-board crystal clock instead of the Time Bus signal.
- loading of the UTC counter with data that is derived from the Time Bus is stopped.
- the UTC counter can be loaded with data that is entered from the VME bus.

If local mode is entered because of missing Time Bus signal, it does not automatically return to normal mode if the Time Bus signal returns. This prevents uncontrolled jumps in the time.

Local mode can be set and cleared from the VME side.
When 'local mode' is cleared and the TIM returns to 'normal mode' (i.e. the Time Bus signal is available), it takes 1 full repetition cycle of the Time Bus signal before a proper UTC decoding takes place. During this time, there is:

- random data loaded into the UTC counter, and
- not proper generation of all the timer clock frequencies (see chapter 4.1.1.).

5.1.2. STATUS REGISTER

This is a 16 bit register with bits for:

- freeze UTC.
- various test signals.
- set/clear local mode.

- UTC interrupt enable (2 bits) for the 10ms and 1 sec interrupt.
- UTC interrupt clear (2 bits) for the 10ms and 1 sec interrupt.

5.1.3. UTC REGISTERS

The UTC registers are latched by the VME 'FREEZEIN' signal.
The following UTC registers are available:

- microseconds (VME read only)
- seconds
- minutes
- hours
- Modified Julian Day

5.1.4. INTERRUPT

The UTC 10 millisec and 1 second can be enabled to generate an interrupt signal to the VME bus. The significant edge of the counter output sets its interrupt flip flop.

5.2. REGISTER ASSIGNMENT

5.2.1. STATUS REGISTER, HIGH BYTE

Location: Base + 0x12, high byte.

D15	D14	D13	D12	D11	D10	D9	D8
FREEZEIN	TBOK	SPARE	LUTC	INHTBL	SETLOC	CLEARLOC	LOCAL

The status after VME SYSRESET is 00 hex.

FREEZEIN	Note: action on rising edge (^).
^	Latching of UTC counter into the UTC registers on falling edge of next UTC counter clock, see chapter 6.4.

TBOK	
0	No Time Bus signal detected (VME read only)
1	Time Bus signal detected (VME read only)

SPARE	
0	Reserved for future use.

LUTC	
0	Normal operation
1	Loading of the UTC counter with data that is stored in the UTC registers (VME write). See notes.

Notes:

- This signal is only effective if 'local' is set.
- The microsecond registers do not have a VME write possibility, the microsecond counters are reset when LUTC is set.
- Loading is performed synchronous on the last TIM board clock pulse (1 MHz) before the LUTC signal is cleared. The setting/clearing of the hardware signal occurs on the falling edge of the TIM board clock pulse.

INHTBL	
0	Normal operation
1	Inhibit the loading of Time Bus data into the UTC counter. Note: this signal is intended for hardware tests.

SETLOC	
0	Normal operation
1	Sets local mode

CLEARLOC	
0	Normal operation
1	Clears local mode.

LOCAL	
0	TIM is in normal mode (VME read only)
1	TIM is in local mode (VME read only)

5.2.2. STATUS REGISTER, LOW BYTE

Location: Base + 0x12, low byte.

D7	D6	D5	D4	D3	D2	D1	D0
SPARE	SPARE	SPARE	SPARE	IENAB7	ICLEAR7	IENAB6	ICLEAR6

The status after VME SYSRESET is 00 hex.

Note: the status of 'INT7' and 'INT6' is accessible via the Interrupt Source Register, see chapter 4.3.5.

IENAB7	
0	Disable 10 millisec interrupts
1	Enable 10 millisec interrupts

ICLEAR7	
0	10 millisec interrupts possible
1	10 millisec interrupts clear

IENAB6	
0	Disable 1 sec interrupts
1	Enable 1 sec interrupts

ICLEAR6	
0	1 sec interrupts possible
1	1 sec interrupts clear

5.2.3. UTC REGISTERS

Reading of the UTC registers must be preceded by a 'FREEZEIN' signal, that causes latching of the momentary value of the UTC counter into registers. Note that the actual latching is delayed, see chapter 6.4.

Writing can be done at any time (except for the microseconds), but the data is only loaded into the UTC counter if:

- the TIM is in local mode, and
- the bit 'LUTC' in the UTC status register is set.

The microsecond counters are reset when these two conditions are true.

This loading is performed synchronous on the last TIM board clock pulse before the LUTC signal is cleared and counting continues from that moment on, see chapter 6.4.

5.2.3.1. Microseconds

The part of the UTC counter that counts the microseconds cannot be loaded from the VME bus, so the UTC registers that contain the microseconds value are VME read only.

The microseconds are counted binary.

Location: Base + 0x18, high byte.

D15	D14	D13	D12	D11	D10	D9	D8
0...							...0

The contents of this byte is always 00 hex.

Location: Base + 0x18, low byte.

D7	D6	D5	D4	D3	D2	D1	D0
MSB...		Microsec's,		high byte			

Location: Base + 0x1a, high byte.

D15	D14	D13	D12	D11	D10	D9	D8
		Microsec's		middle byte			

Location: Base + 0x1a, low byte.

D7	D6	D5	D4	D3	D2	D1	D0
		Microsec's,		low byte			...LSB

The status of the 3 microseconds bytes after VME SYSRESET is 0. Reset occurs also at the change of the UTC second or by loading of the UTC counter from the VME bus with the signal 'LUTC'.

5.2.3.2. Seconds

The seconds are counted in BCD format.

Location: Base + 0x1c, low byte

D7	D6	D5	D4	D3	D2	D1	D0
Seconds, tens BCD				Seconds, units BCD			

The status after VME SYSRESET is 0, a new state is entered at:

- VME writing, or
- the first Time Bus data loading after SYSRESET.

5.2.3.3. Minutes

The minutes are counted in BCD format.

Location: Base + 0x1c, high byte

D15	D14	D13	D12	D11	D10	D9	D8
Minutes, tens BCD				Minutes, units BCD			

The status after VME SYSRESET is 0, a new state is entered at:

- VME writing, or
- the first Time Bus data loading after SYSRESET.

5.2.3.4. Hours

The hours are counted in BCD format.

Location: Base + 0x1e, low byte

D7	D6	D5	D4	D3	D2	D1	D0
Hours, tens BCD				Hours, units BCD			

The status after VME SYSRESET is 0, a new state is entered at:

- VME writing, or
- the first Time Bus data loading after SYSRESET.

5.2.3.5. Modified Julian Day

The MJD is counted in BCD format. The Time Bus distributes 5 BCD digits.

Note 1: MJD is principally related to UT1. UT1 has variable difference of less than 1 second compared to UTC. The MJD changes therefore not at midnight UTC. However, because of the fact that the whole VLT system is based on UTC and because MJD should also be incremented in local mode, MJD is incremented at midnight UTC.

Note 2: The Modified Julian Date is a float number, scaled in days. The MJD which is distributed by the Time Bus is an integer and is therefore called Modified Julian Day.

Location: Base + 0x20, high byte

D15	D14	D13	D12	D11	D10	D9	D8
0...							...0

The contents of this byte is always 00 hex.

Location: Base + 0x20, low byte

D7	D6	D5	D4	D3	D2	D1	D0
Modif. Julian Day, high byte (D7 through D4 are always 0; D3 through D0 contain 1 BCD digit							

Location: Base + 0x22, high byte

D15	D14	D13	D12	D11	D10	D9	D8
Modif. Julian Day, middle byte (2 BCD digits)							

Location: Base + 0x22, low byte

D7	D6	D5	D4	D3	D2	D1	D0
Modif. Julian Day, low byte (2 BCD digits)							

The status of these bytes after VME SYSRESET is 0, a new state is entered at:

- VME writing, or
- the first Time Bus data loading after SYSRESET.

6. PRINCIPLES OF OPERATION

6.1. VME BUS INTERFACE

6.1.1. VME INTERRUPTER

Each of the 8 possible interrupt sources (6 timers, 1 Hz and 100 Hz from the UTC) can trigger a flipflop if the corresponding interrupt enable bit is set.

Each interrupt has to be cleared by pulsing (setting and clearing) the Interrupt Clear bit, which clears the interrupt flip flop. This has to be done by the interrupt service routine (Release On Register Access, RORA).

6.2. TIMER GATING

In the gating modes 'clear gate', 'hardware gate' and 'set gate', the selected gate signal and the selected clock frequency are directly fed to the timer.

6.2.1. GATING ON 'NEXT 100 MILLISECOND'

The programming sequence as described in chapter 4.1.2. has to be followed.

Just before the end of the current 100 millisecond, the hardware signal 'DOTX99' is generated. This signal sets a flip flop if 'gate next 100 millisecond' is selected.
In this way, there is always a clock pulse of 0.5 us just before the 1 second edge, irrespective of the selected clock frequency.
The falling edge of the pulse (which is at the 100 millisecond edge) loads the timer. From that moment on, clock pulses are fed to the timer.

6.3. UTC READING

The VME 'FREEZEIN' signal is clocked with the falling edge (i.e. the non-significant edge) of the 1 MHz counting clock. This allows the UTC counter to settle before it is latched.
Result is that the hardware 'FREEZE' signal has a delay that varies between 0 and 1 microsecond.

6.4. UTC WRITING

In normal operation, the UTC which is decoded from the Time Bus is loaded into the UTC counter. This operation is repeated every second.

In local mode, the UTC can be loaded via the VME bus.
The first step of writing to the UTC counter is to write data to the UTC registers. This does not yet load the data into the UTC counter.
Then, pulsing (set and then clear) the VME signal 'LUTC' loads this data synchronously for all registers. The actual loading is always in at a different time than the 1MHz UTC counter clock. This is to respect the set-up and hold times of the counter: the hardware load signal changes state on the falling edge of the clock only, while loading occurs on the rising edge.

The board access time is set to 1.2 microsec. By this, pulsing 'LUTC' can be done in 2 subsequent VME accesses: there will always be a rising clock edge in between to load the counter, even with a very fast CPU.

6.5. TIME BUS DECODING

The Time Bus signal is a serial coded signal based on the IRIG-B coding scheme. The modulation is however completely different:
The signal is a (fiber optic) digital pulse width modulated (PWM) signal with a carrier frequency of 1MHz. The bit value '0' corresponds with a duty cycle of 20%, while a '1' corresponds with a 80% duty cycle. The 1MHz carrier is locked in a Phase Locked Loop. This PLL generates a TBCLK signal with 50% duty cycle, which is used throughout the TIM as synchronous clock signal '1MHZ'. The falling edge of this signal is used to clock the data bit. As the IRIG-B code is based on a bit time of 1 millisec, the shift of the data into the shift register (serial to parallel converter) is done with this frequency.
As soon as a part of the time frame is decoded, a corresponding load pulse is generated. This loads the decoded part into the UTC counter. The loading occurs at the first microsecond after the corresponding field in the IRIG-B code frame.

The 'PLL locked' signal is used as TBOK signal. When the Time Bus signal is lost, TBOK will go low about 12 microsec after the last Time Bus pulse. This sets LOCAL. TBCLK will drift only < 0.5 microsec during this time interval. A quartz oscillator will continue to provide an accurate 1MHz signal as soon as TBOK goes low, see the timing diagram.

7. DRAWINGS

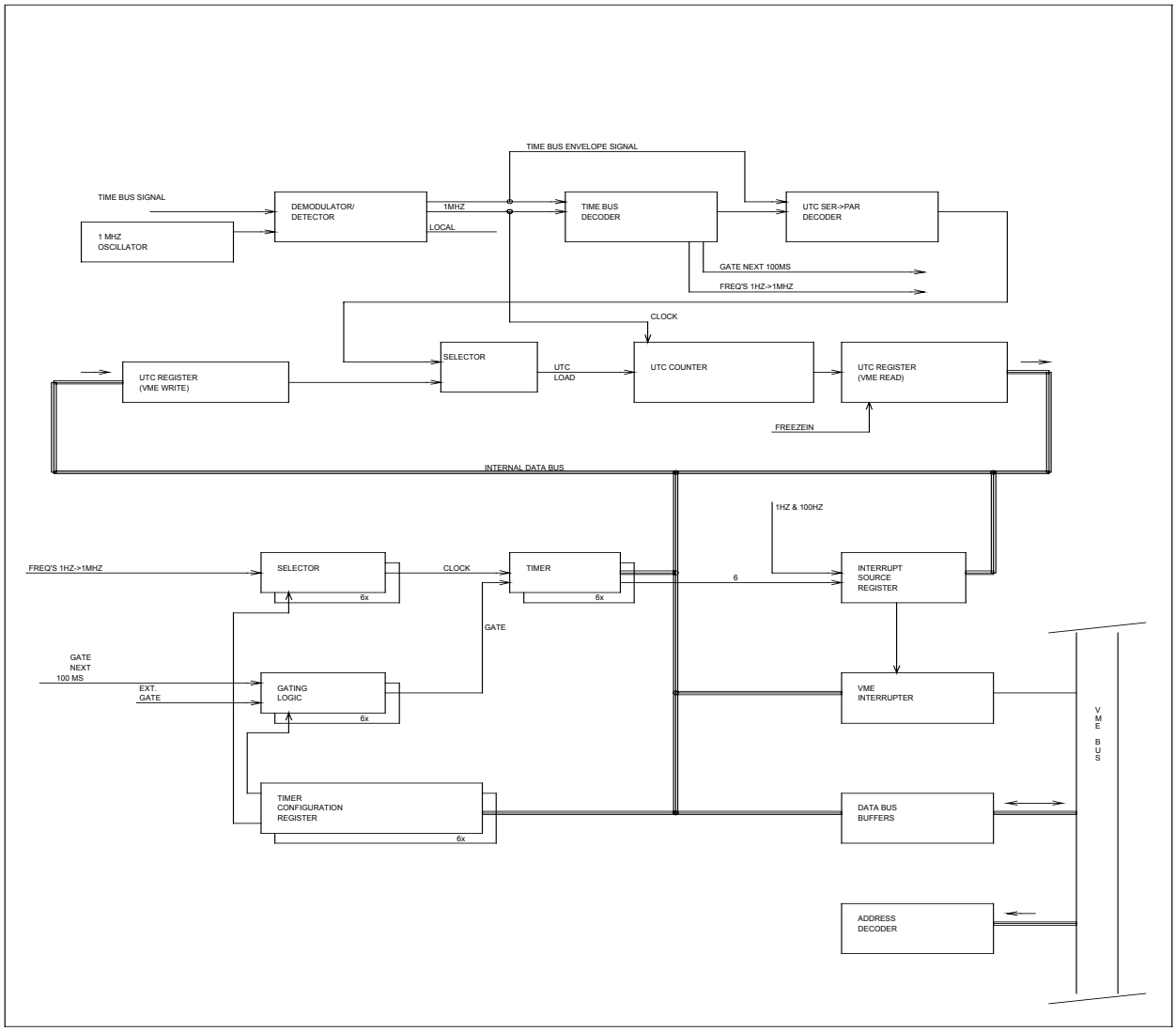


Fig. 6 TIM block diagram.

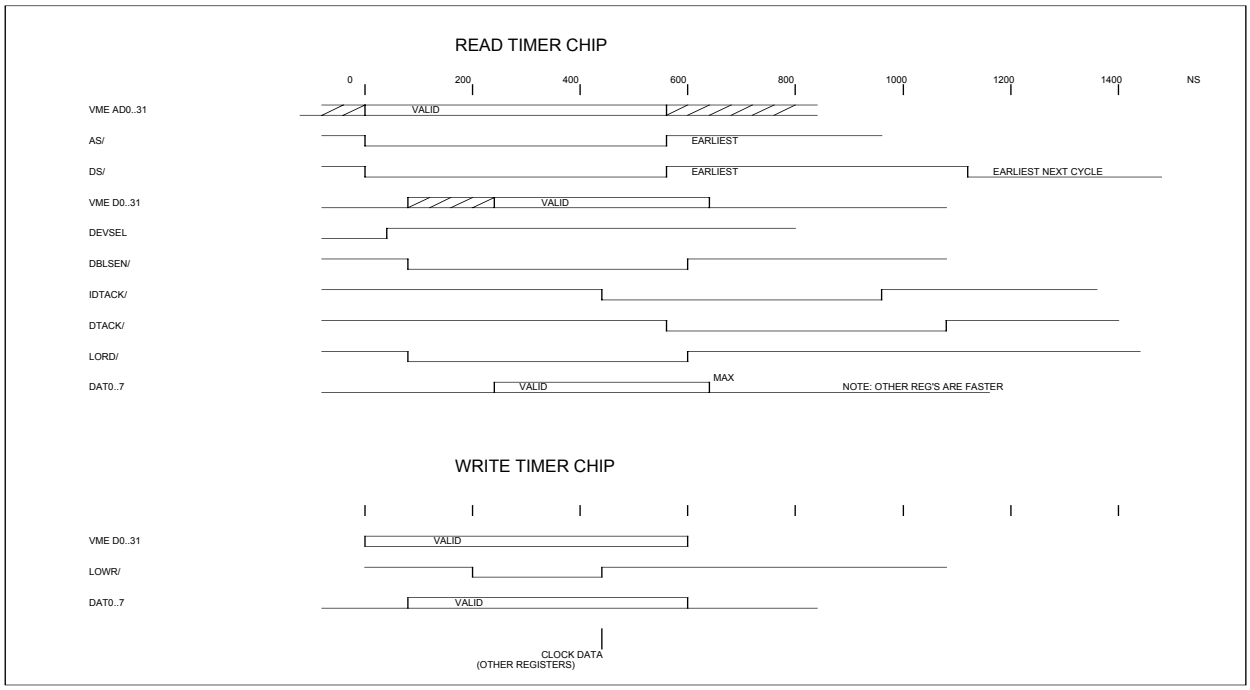


Fig. 7 VME read / write timing.

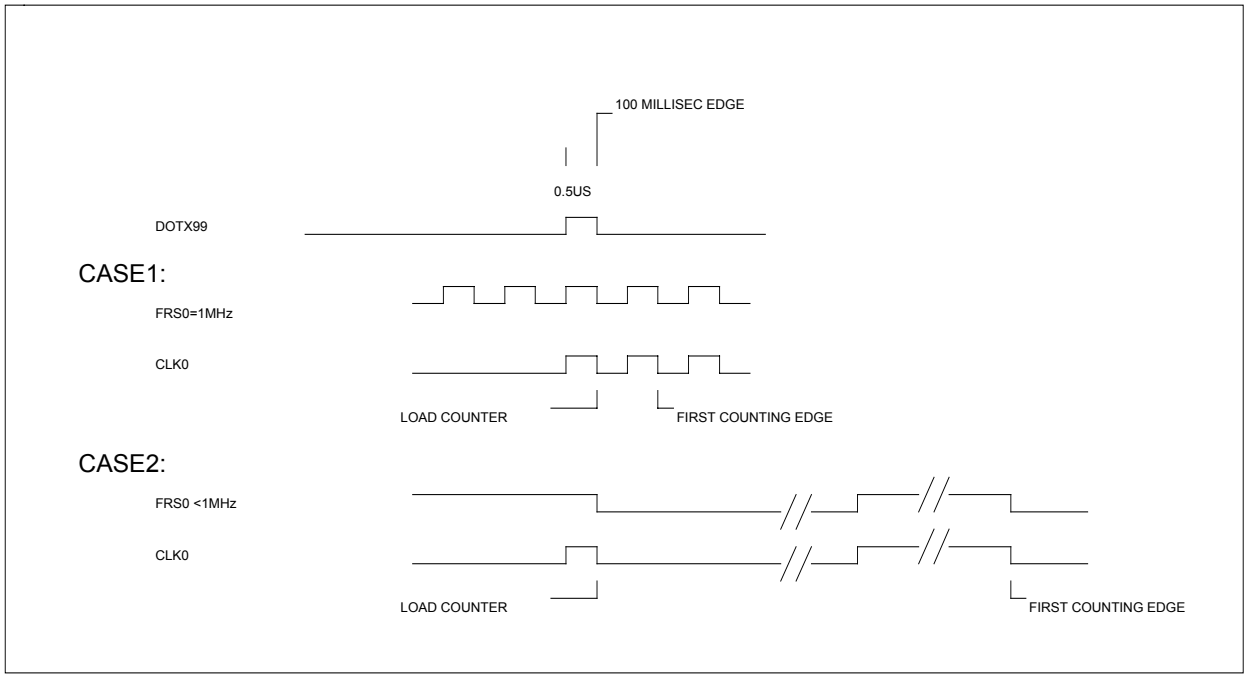


Fig. 8 Timing for 'gate next 100 millisecond'.

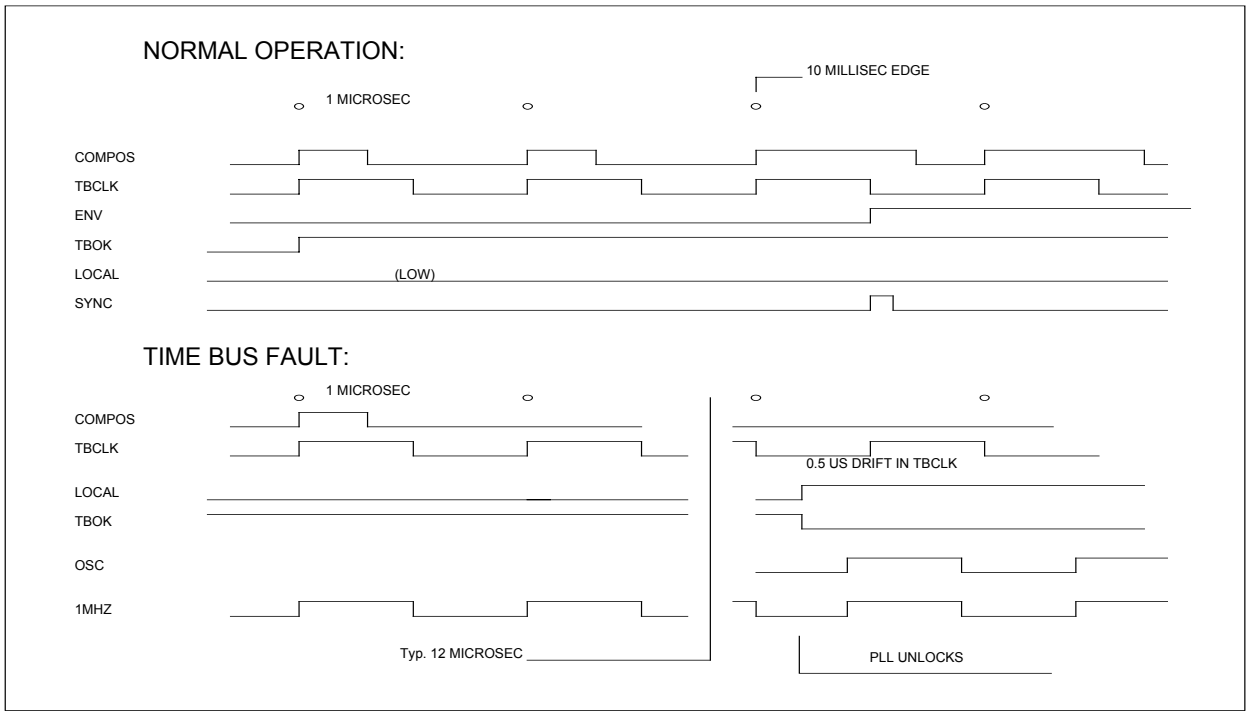


Fig. 9 UTC composite decoding.

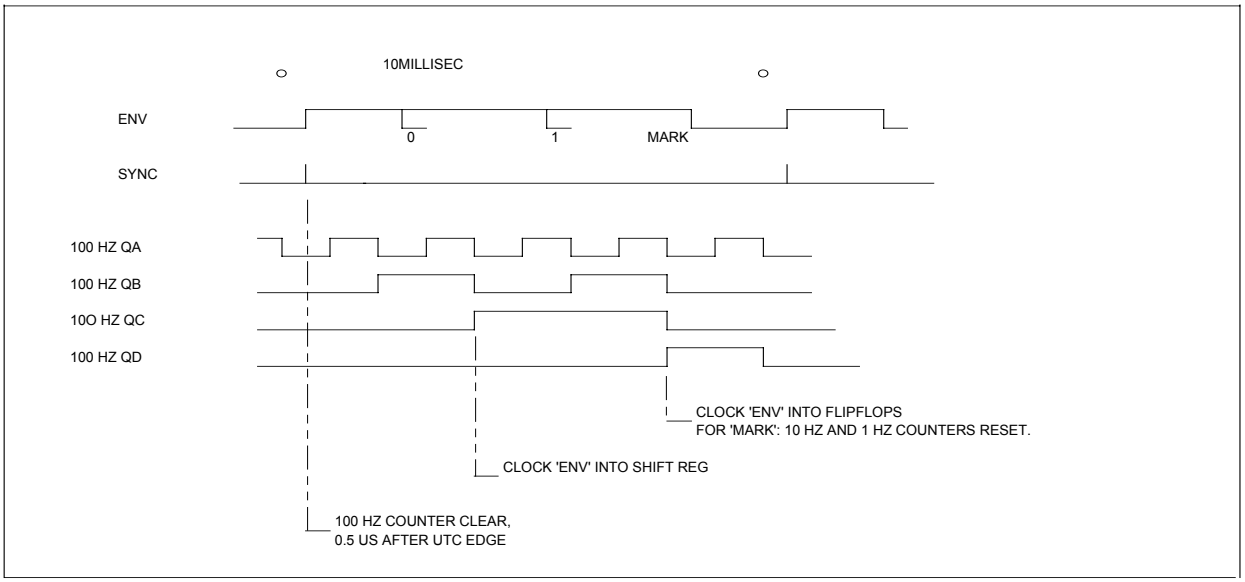


Fig. 10 UTC 10 millisecond decoding.

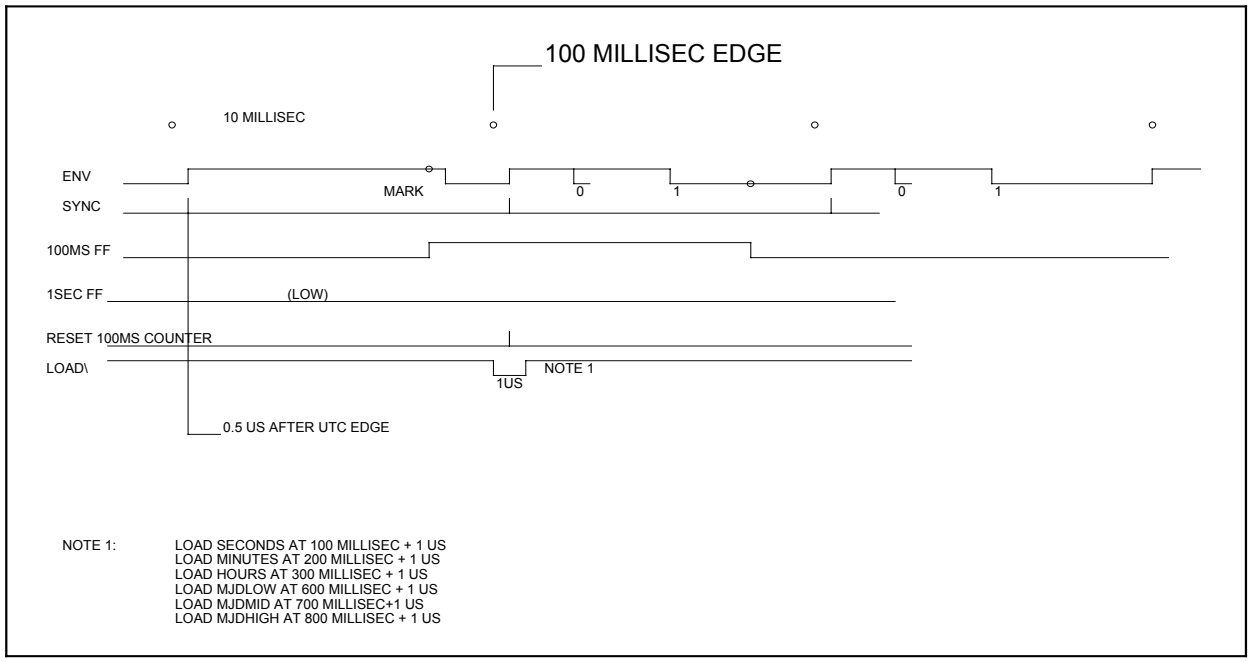


Fig. 11 UTC 100 millisec decoding.

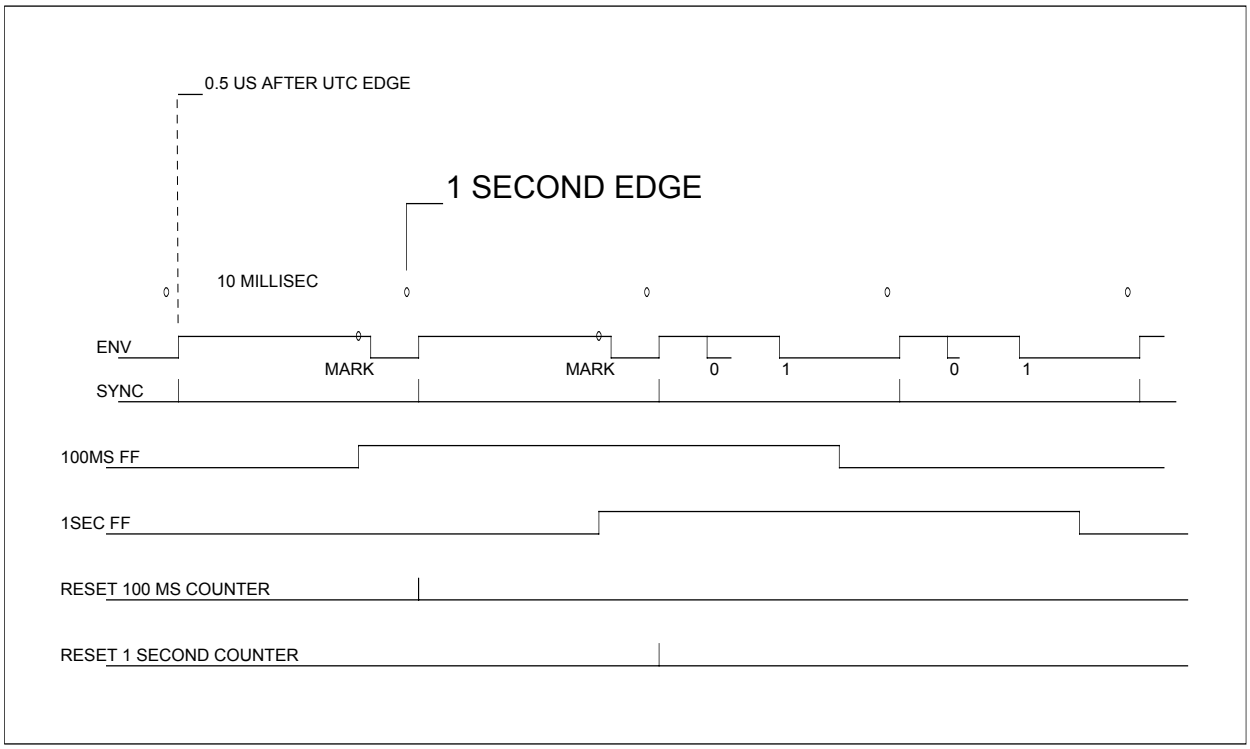


Fig. 12 UTC 1 second decoding.

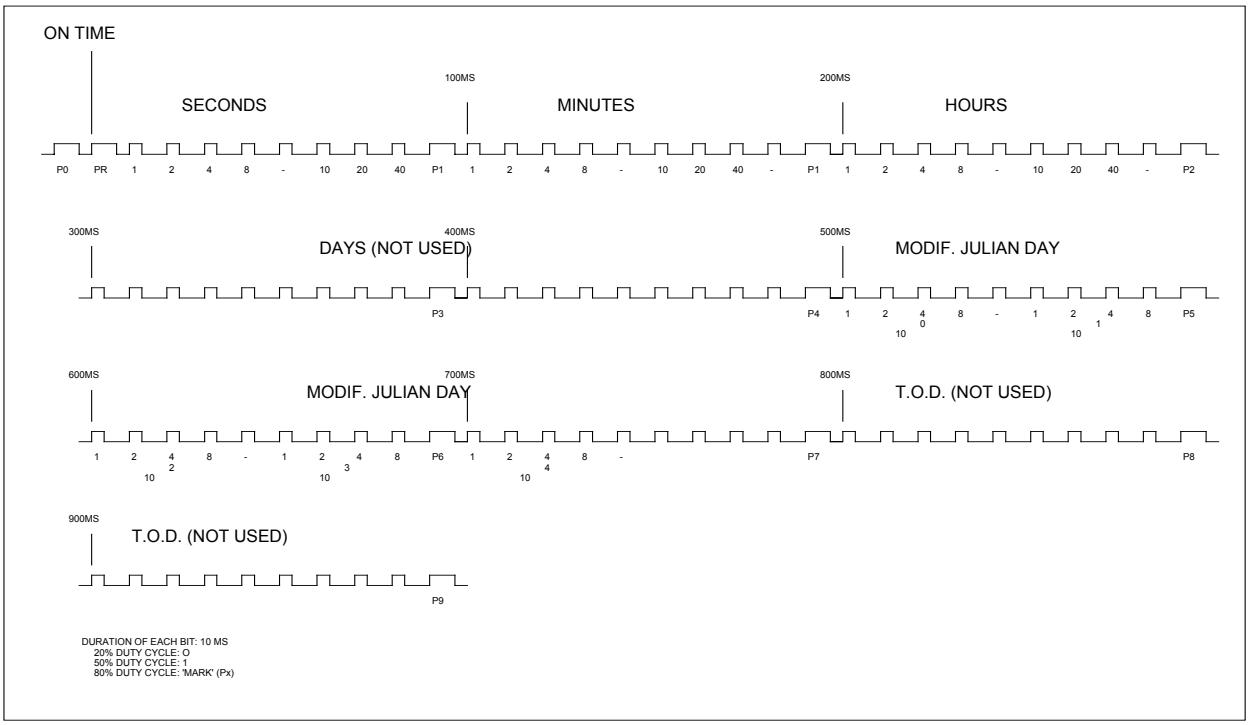


Fig. 13 IRIG-B code format.

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