

LOW VOLTAGE 4 Megabit (256K x 16) UV EPROM and OTP EPROM

PRELIMINARY DATA

- LOW VOLTAGE READ OPERATION:
3V to 5.5V
- FAST ACCESS TIME: 120ns
- LOW POWER "CMOS" CONSUMPTION:
 - Active Current 15mA
 - Standby Current 20 μ A
- PROGRAMMING VOLTAGE: 12.75V
- PROGRAMMING TIMES of AROUND 24sec.
(PRESTO II ALGORITHM)
- M27V402 is PROGRAMMABLE as M27C4002
with IDENTICAL SIGNATURE

DESCRIPTION

The M27V402 is a low voltage, low power 4 Megabit UV erasable and electrically programmable EPROM, ideally suited for handheld and portable microprocessor systems requiring large programs. It is organized as 262,144 by 16 bits.

The M27V402 operates in the read mode with a supply voltage as low as 3V. The decrease in operating power allows either a reduction of the size of the battery or an increase in the time between battery recharges.

The M27V402 can also be operated as a standard 4 Megabit EPROM (similar to M27C4002) with a 5V power supply.

Table 1. Signal Names

A0 - A17	Address Inputs
Q0 - Q15	Data Outputs
\bar{E}	Chip Enable
\bar{G}	Output Enable
V _{PP}	Program Supply
V _{CC}	Supply Voltage
V _{SS}	Ground

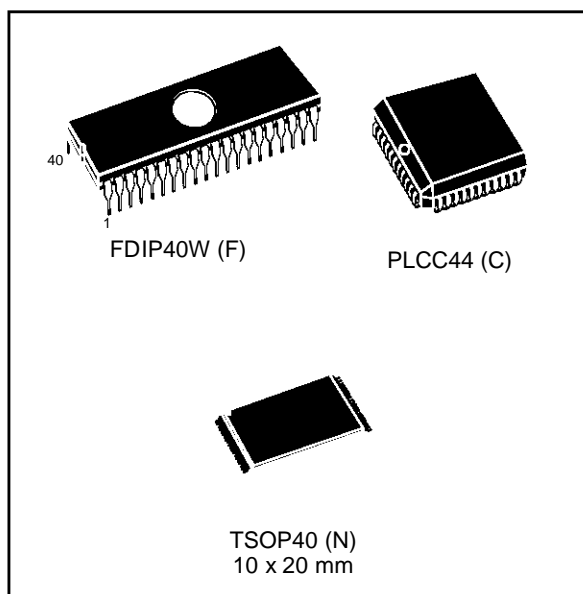


Figure 1. Logic Diagram

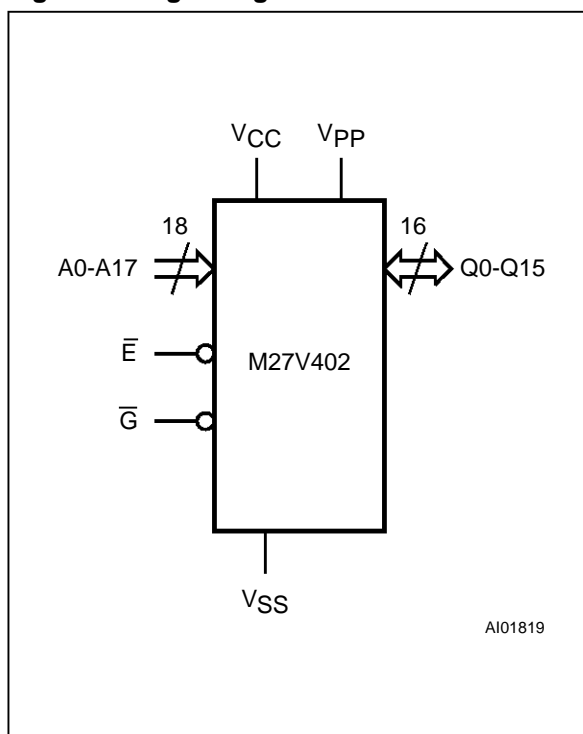


Figure 2A. DIP Pin Connections

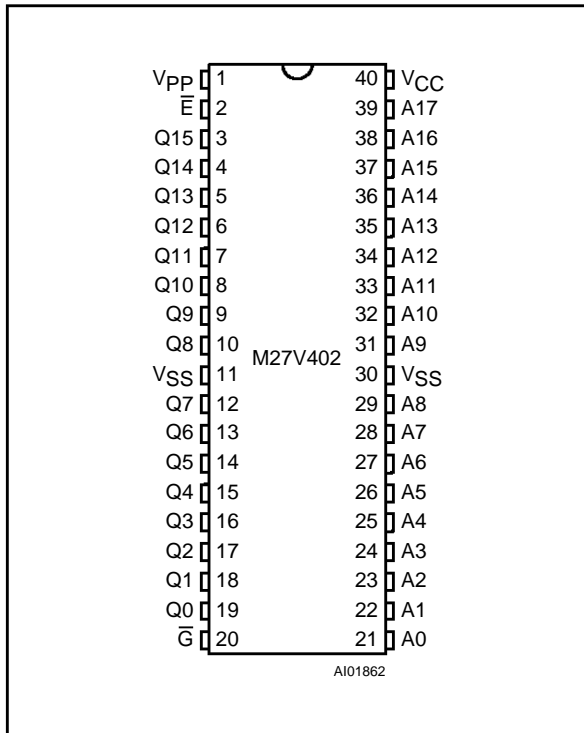
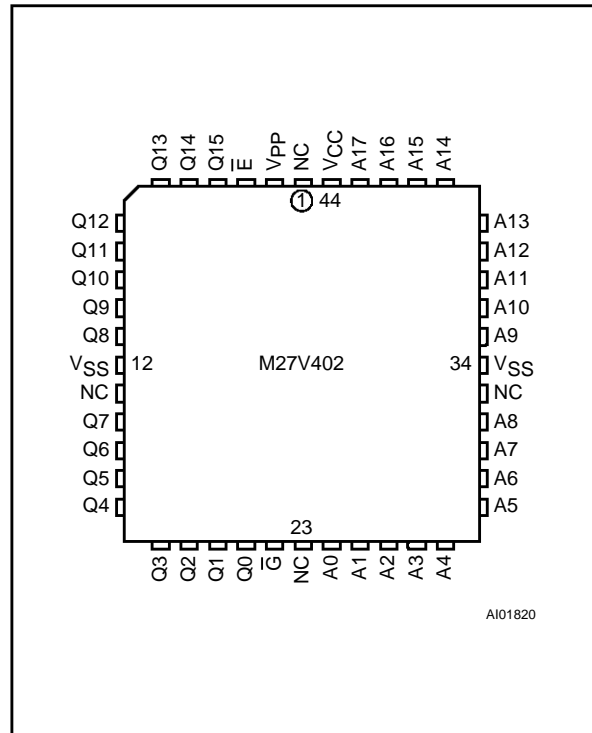
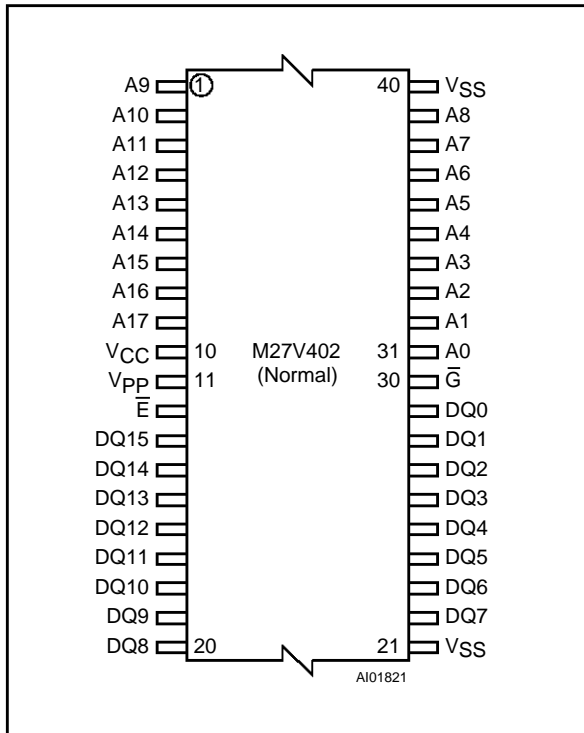


Figure 2B. LCC Pin Connections



Warning: NC = Not Connected.

Figure 2C. TSOP Pin Connections



DESCRIPTION (cont'd)

The Window Ceramic Frit-Seal Dual-in-Line package has transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure. For applications where the content is programmed only one time and erasure is not required, the M27V402 is offered in both Plastic Leaded Chip Carrier and Plastic thin Small Outline packages.

DEVICE OPERATION

The modes of operations of the M27V402 are listed in the Operating Modes table. A single power supply is required in the read mode. All inputs are TTL levels except for V_{pp} and 12V on A9 for Electronic Signature.

Read Mode

The M27V402 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable (\bar{E}) is the power control and should be used for device selection. Output Enable (\bar{G}) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the

Table 2. Absolute Maximum Ratings ⁽¹⁾

Symbol	Parameter	Value	Unit
T _A	Ambient Operating Temperature	-40 to 125	°C
T _{BIAS}	Temperature Under Bias	-50 to 125	°C
T _{STG}	Storage Temperature	-65 to 150	°C
V _{IO} ⁽²⁾	Input or Output Voltages (except A9)	-2 to 7	V
V _{CC}	Supply Voltage	-2 to 7	V
V _{A9} ⁽²⁾	A9 Voltage	-2 to 13.5	V
V _{PP}	Program Supply Voltage	-2 to 14	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

2. Minimum DC voltage on Input or Output is -0.5V with possible undershoot to -2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

Table 3. Operating Modes

Mode	\bar{E}	\bar{G}	A9	V _{PP}	Q0 - Q15
Read	V _{IL}	V _{IL}	X	V _{CC} or V _{SS}	Data Out
Output Disable	V _{IL}	V _{IH}	X	V _{CC} or V _{SS}	Hi-Z
Program	V _{IL} Pulse	V _{IH}	X	V _{PP}	Data In
Verify	V _{IH}	V _{IL}	X	V _{PP}	Data Out
Program Inhibit	V _{IH}	V _{IH}	X	V _{PP}	Hi-Z
Standby	V _{IH}	X	X	V _{CC} or V _{SS}	Hi-Z
Electronic Signature	V _{IL}	V _{IL}	V _{ID}	V _{CC}	Codes

Note: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V _{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V _{IH}	0	1	0	0	0	1	0	0	44h

addresses are stable, the address access time (t_{AVQV}) is equal to the delay from \bar{E} to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of \bar{G} , assuming that \bar{E} has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27V402 has a standby mode which reduces the active current from 20mA to 20μA with low

voltage operation V_{CC} ≤ 3.3V (50mA to 100μA with a supply of 5.5V), see Read Mode DC Characteristics table for details. The M27V402 is placed in the standby mode by applying a CMOS high signal to the \bar{E} input. When in the standby mode, the outputs are in a high impedance state, independent of the \bar{G} input.

Table 5. AC Measurement Conditions

	High Speed	Standard
Input Rise and Fall Times	≤ 10ns	≤ 20ns
Input Pulse Voltages	0 to 3V	0.45V to 2.4V
Input and Output Timing Ref. Voltages	1.5V	0.8V and 2V

Figure 3. AC Testing Input Output Waveform

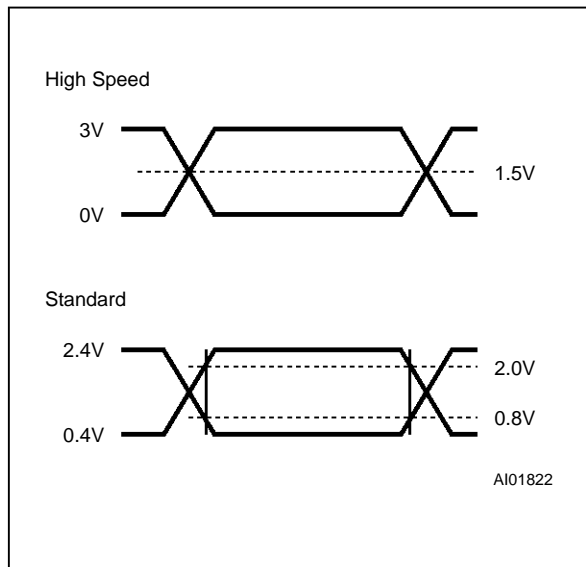


Figure 4. AC Testing Load Circuit

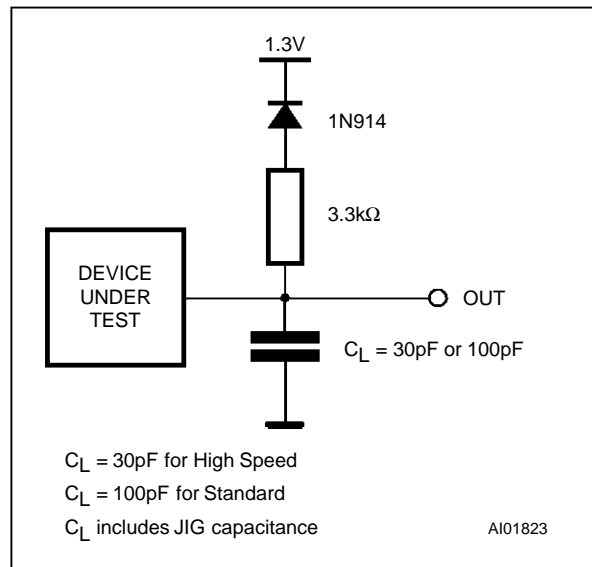


Table 6. Capacitance⁽¹⁾ (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V		6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

- a. the lowest possible memory power dissipation,
- b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, \overline{E} should be decoded and used as the primary device selecting function, while \overline{G} should be made a common connection to all devices in the array and connected to the READ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

Table 7. Read Mode DC Characteristics ⁽¹⁾(T_A = 0 to 70°C, –20 to 70°C, –20 to 85°C or –40 to 85°C; V_{CC} = 3.3V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I _{LI}	Input Leakage Current	0V ≤ V _{IN} ≤ V _{CC}		±10	μA
I _{LO}	Output Leakage Current	0V ≤ V _{OUT} ≤ V _{CC}		±10	μA
I _{CC}	Supply Current	$\bar{E} = V_{IL}, \bar{G} = V_{IL}, I_{OUT} = 0mA, f = 5MHz, V_{CC} = 3.2V$		20	mA
		$\bar{E} = V_{IL}, \bar{G} = V_{IL}, I_{OUT} = 0mA, f = 5MHz, V_{CC} = 5.5V$		50	mA
I _{CC1}	Supply Current (Standby) TTL	$\bar{E} = V_{IH}$		1	mA
I _{CC2}	Supply Current (Standby) CMOS	$\bar{E} > V_{CC} - 0.2V, V_{CC} = 3.2V$		20	μA
		$\bar{E} > V_{CC} - 0.2V, V_{CC} = 5.5V$		100	μA
I _{PP}	Program Current	V _{PP} = V _{CC}		10	μA
V _{IL}	Input Low Voltage		–0.3	0.8	V
V _{IH} ⁽²⁾	Input High Voltage		2	V _{CC} + 1	V
V _{OL}	Output Low Voltage	I _{OL} = 2.1mA		0.4	V
V _{OH}	Output High Voltage TTL	I _{OH} = –400μA	2.4		V
	Output High Voltage CMOS	I _{OH} = –100μA	V _{CC} – 0.7V		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Maximum DC voltage on Output is V_{CC} + 0.5V.

System Considerations

The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of \bar{E} . The magnitude of the transient current peaks is dependent on the output capacitive and inductive loading of the device.

The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1μF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7μF bulk electrolytic capacitor should be used

between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

When delivered (and after each erasure for UV EPROM), all bits of the M27V402 are in the "1" state. Data is introduced by selectively programming "0"s into the desired bit locations. Although only "0"s will be programmed, both "1"s and "0"s can be present in the data word. The only way to change a "0" to a "1" is by die exposure to ultraviolet light (UV EPROM). The M27V402 is in the programming mode when V_{PP} input is at 12.75V, \bar{G} is at V_{IH} and \bar{E} is pulsed to V_{IL}. The data to be programmed is applied to 16 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25V.

Table 8. Read Mode AC Characteristics ⁽¹⁾

($T_A = 0$ to 70°C , -20 to 70°C , -20 to 85°C or -40 to 85°C ; $V_{CC} = 3.3\text{V} \pm 10\%$; $V_{PP} = V_{CC}$)

Symbol	Alt	Parameter	Test Condition	M27V402						Unit
				-120 ⁽³⁾		-150		-200		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\bar{E} = V_{IL}, \bar{G} = V_{IL}$		120		150		200	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\bar{G} = V_{IL}$		120		150		200	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\bar{E} = V_{IL}$		60		80		100	ns
$t_{EHQZ}^{(2)}$	t_{DF}	Chip Enable High to Output Hi-Z	$\bar{G} = V_{IL}$	0	50	0	50	0	50	ns
$t_{GHQZ}^{(2)}$	t_{DF}	Output Enable High to Output Hi-Z	$\bar{E} = V_{IL}$	0	50	0	50	0	50	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\bar{E} = V_{IL}, \bar{G} = V_{IL}$	0		0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP} .

2. Sampled only, not 100% tested.

3. In case of 120ns speed see High Speed AC Measurement conditions.

Figure 5. Read Mode AC Waveforms

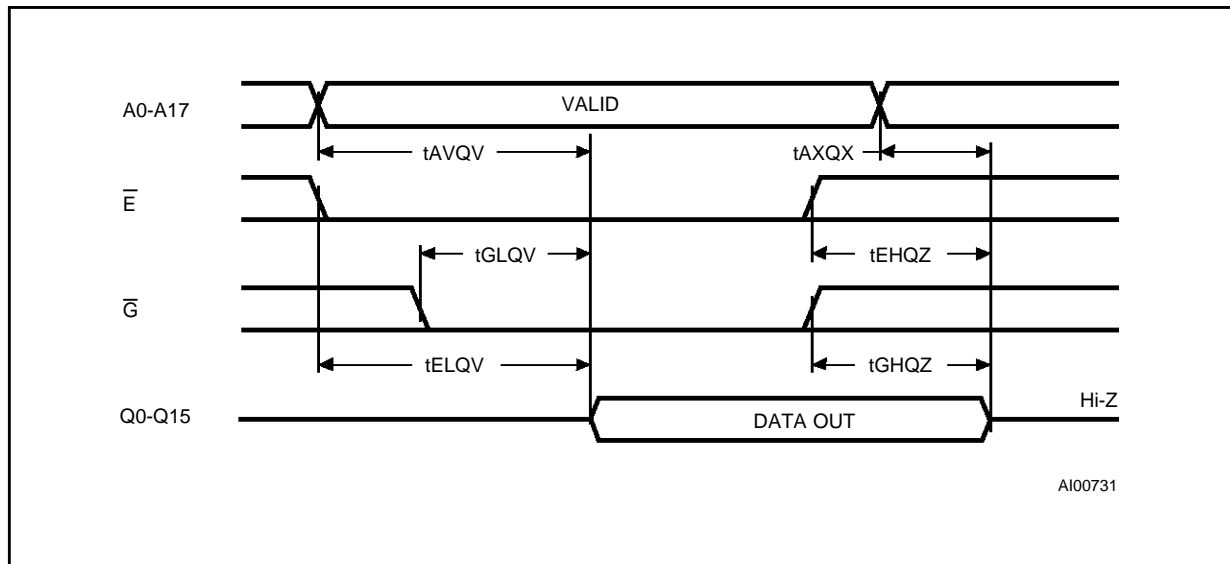


Table 9. Programming Mode DC Characteristics ⁽¹⁾(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I _{LI}	Input Leakage Current	0 ≤ V _{IN} ≤ V _{CC}		±10	μA
I _{CC}	Supply Current			50	mA
I _{PP}	Program Current	$\bar{E} = V_{IL}$		50	mA
V _{IL}	Input Low Voltage		-0.3	0.8	V
V _{IH}	Input High Voltage		2	V _{CC} + 0.5	V
V _{OL}	Output Low Voltage	I _{OL} = 2.1mA		0.4	V
V _{OH}	Output High Voltage TTL	I _{OH} = -400μA	2.4		V
V _{ID}	A9 Voltage		11.5	12.5	V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.**Table 10. Programming Mode AC Characteristics ⁽¹⁾**(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t _{AVEL}	t _{AS}	Address Valid to Chip Enable Low		2		μs
t _{QVEL}	t _{DS}	Input Valid to Chip Enable Low		2		μs
t _{VPHEL}	t _{VPS}	V _{PP} High to Chip Enable Low		2		μs
t _{VCHL}	t _{VCS}	V _{CC} High to Chip Enable Low		2		μs
t _{ELEH}	t _{PW}	Chip Enable Program Pulse Width		95	105	μs
t _{EHQX}	t _{DH}	Chip Enable High to Input Transition		2		μs
t _{QXGL}	t _{OES}	Input Transition to Output Enable Low		2		μs
t _{GLQV}	t _{OE}	Output Enable Low to Output Valid			100	ns
t _{GHQZ}	t _{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t _{GHAX}	t _{AH}	Output Enable High to Address Transition		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Figure 6. Programming and Verify Modes AC Waveforms

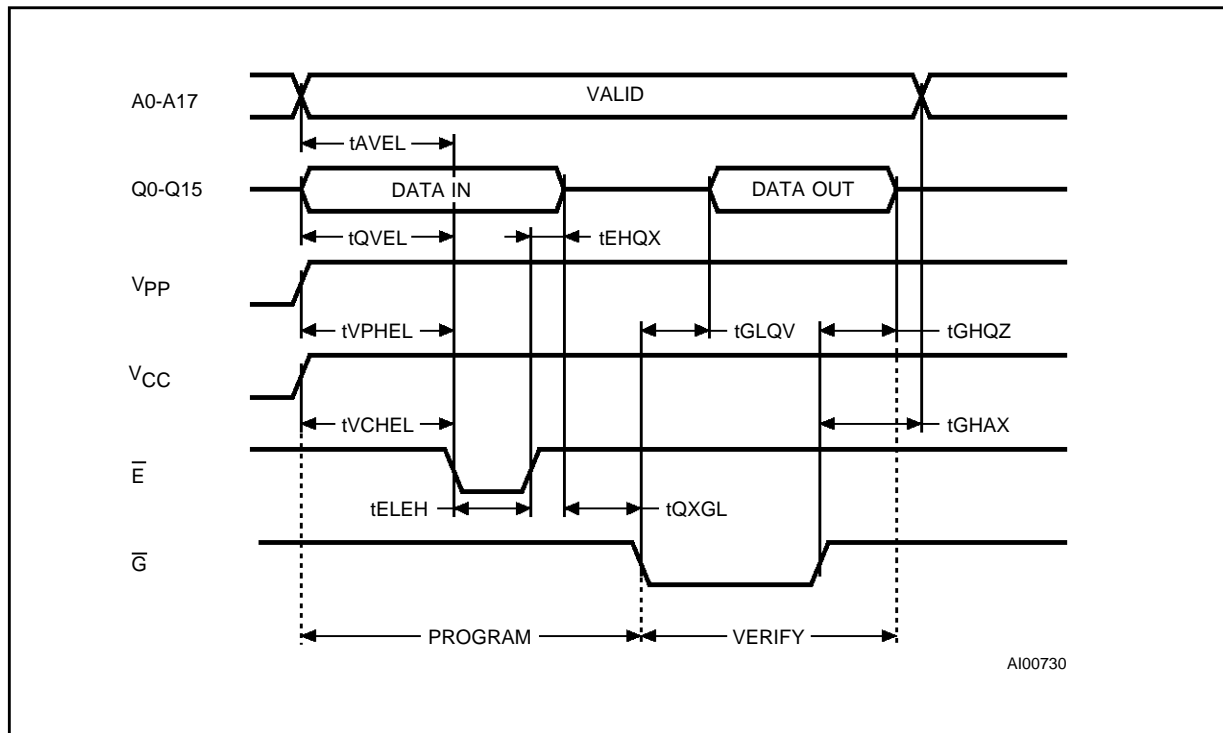
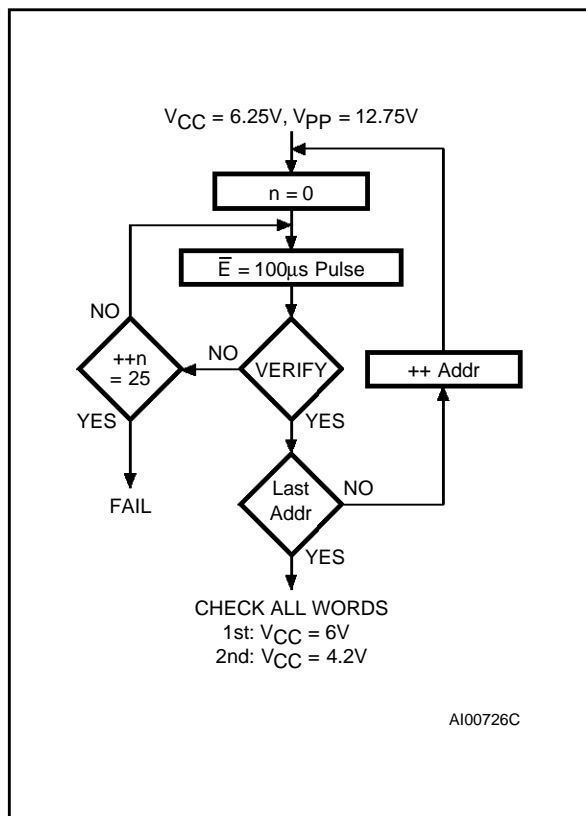


Figure 7. Programming Flowchart



PRESTO II Programming Algorithm

PRESTO II Programming Algorithm allows the whole array to be programmed with a guaranteed margin, in a typical time of 26.5 seconds. Programming with PRESTO II consists of applying a sequence of 100µs program pulses to each byte until a correct verify occurs (see Figure 7). During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides necessary margin to each programmed cell.

Program Inhibit

Programming of multiple M27V402s in parallel with different data is also easily accomplished. Except for \bar{E} , all like inputs including \bar{G} of the parallel M27V402 may be common. A TTL low level pulse applied to a M27V402's \bar{E} input, with VPP at 12.75V, will program that M27V402. A high level \bar{E} input inhibits the other M27V402s from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with \bar{G} at V_{IL} , \bar{E} at V_{IH} , VPP at 12.75V and VCC at 6.25V.

On-Board Programming

The M27V402 can be directly programmed in the application circuit. See the relevant Application Note AN620.

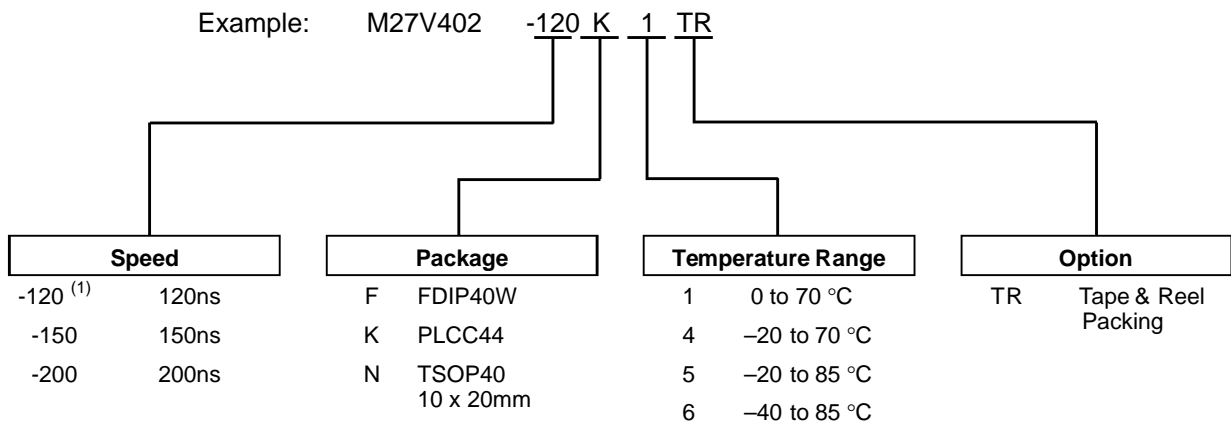
Electronic Signature

The Electronic Signature (ES) mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. The ES mode is functional in the $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ ambient temperature range that is required when programming the M27V402. To activate the ES mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27V402 with $V_{PP}=V_{CC}=5\text{V}$. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH} . All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 ($A0=V_{IL}$) represents the manufacturer code and byte 1 ($A0=V_{IH}$) the device identifier code. For the SGS-THOMSON M27V402, these two identifier bytes are given in Table 4 and can be read-out on outputs Q0 to Q7.

ERASURE OPERATION (applies to UV EPROM)

The erasure characteristics of the M27V402 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000\AA . It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the $3000\text{-}4000\text{\AA}$ range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27V402 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27V402 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27V402 window to prevent unintentional erasure. The recommended erasure procedure for the M27V402 is exposure to short wave ultraviolet light which has a wavelength of 2537\AA . The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2 . The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with $12000\text{ }\mu\text{W/cm}^2$ power rating. The M27V402 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION SCHEME



Note: 1. High Speed, see AC Characteristics section for further information.

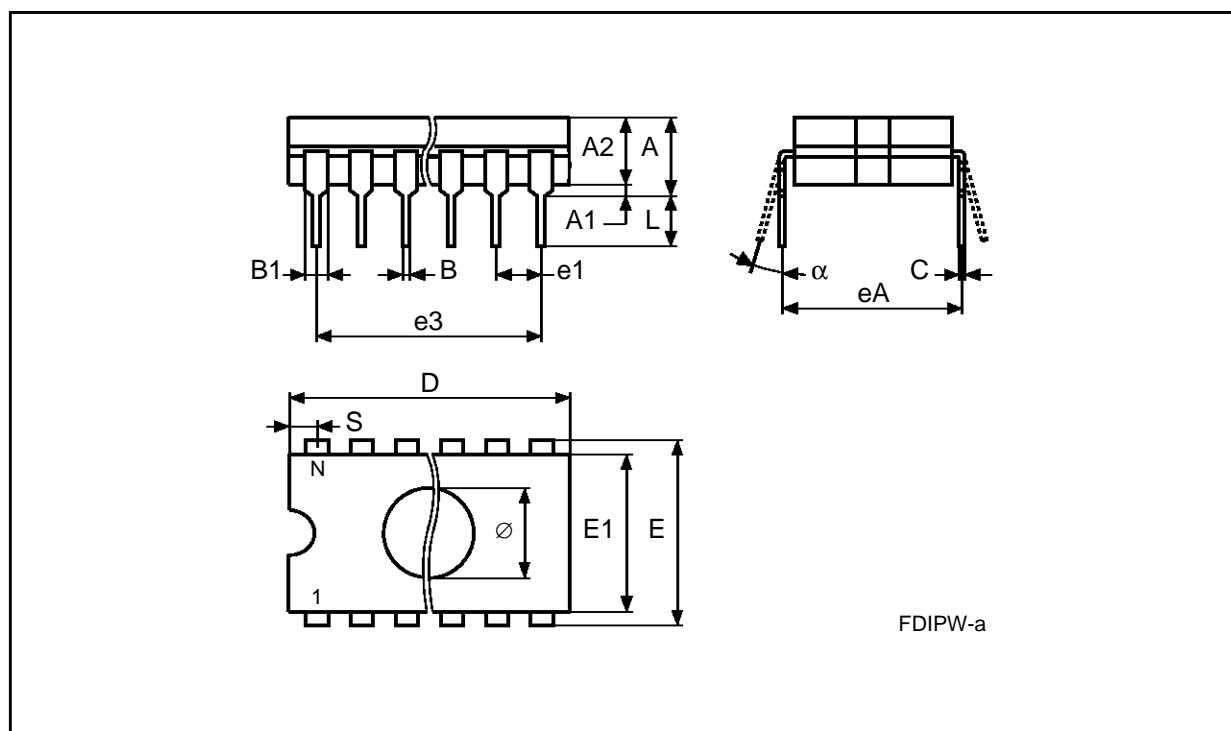
For a list of available options (Speed, V_{CC} Tolerance, Package etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

FDIP40W - 40 pin Ceramic Frit-seal DIP, with window

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			5.71			0.225
A1		0.50	1.78		0.020	0.070
A2		3.90	5.08		0.154	0.200
B		0.40	0.55		0.016	0.022
B1		1.27	1.52		0.050	0.060
C		0.22	0.31		0.009	0.012
D			53.40			2.102
E		15.40	15.80		0.606	0.622
E1		13.10	13.50		0.514	0.530
e1	2.54	–	–	0.100	–	–
e3	48.26	–	–	1.900	–	–
eA		16.17	18.32		0.637	0.721
L		3.18	4.10		0.125	0.161
S		1.52	2.49		0.060	0.098
	8.13	–	–	0.320	–	–
α		4	15		4	15
N		40			40	

FDIP40W

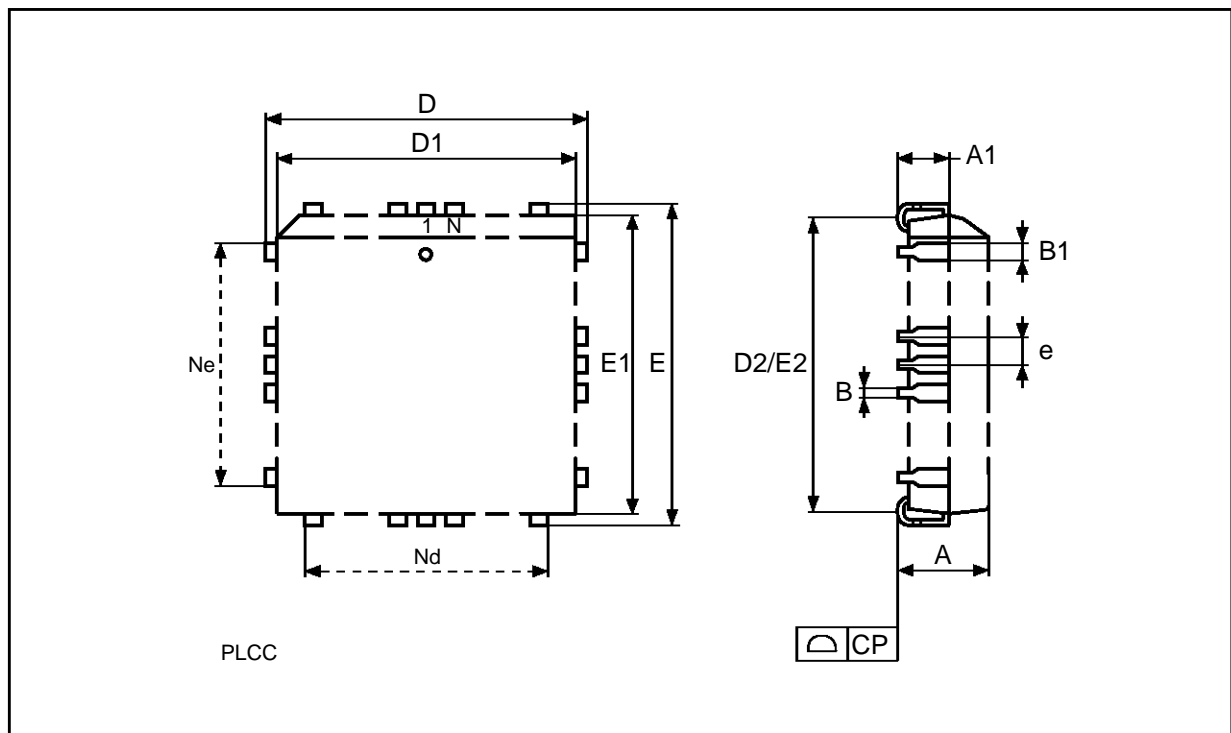


Drawing is not to scale

PLCC44 - 44 lead Plastic Leaded Chip Carrier, square

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		4.20	4.70		0.165	0.185
A1		2.29	3.04		0.090	0.120
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		17.40	17.65		0.685	0.695
D1		16.51	16.66		0.650	0.656
D2		14.99	16.00		0.590	0.630
E		17.40	17.65		0.685	0.695
E1		16.51	16.66		0.650	0.656
E2		14.99	16.00		0.590	0.630
e	1.27	-	-	0.050	-	-
N	44			44		
CP			0.10			0.004

PLCC44

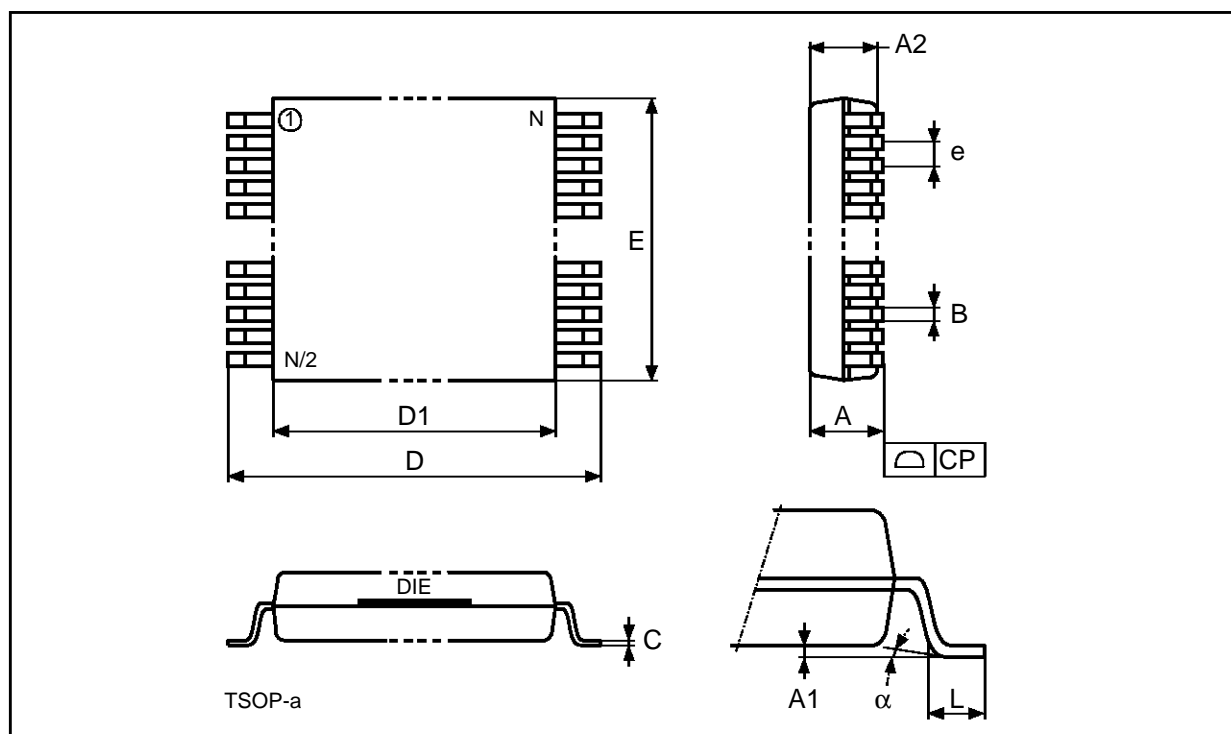


Drawing is not to scale

TSOP40 - 40 lead Plastic Thin Small Outline, 10 x 20mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.05	0.15		0.002	0.006
A2		0.95	1.05		0.037	0.041
B		0.17	0.27		0.007	0.011
C		0.10	0.21		0.004	0.008
D		19.80	20.20		0.780	0.795
D1		18.30	18.50		0.720	0.728
E		9.90	10.10		0.390	0.398
e	0.50	-	-	0.020	-	-
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N	40			40		
CP			0.10			0.004

TSOP40



Drawing is not to scale

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