XC7272A
72-Macrocell CMOS CPLD

June 1, 1996 (Version 1.0) | Product Specification

Features

- Second-Generation High Density Programmable Logic Device
- UV-erasable CMOS EPROM technology
- 72 macrocells, grouped into eight Function Blocks (FBs), interconnected by a programmable Universal Interconnect Matrix
- Each FB contains a programmable AND-array with 21 complementary inputs, providing up to 16 product terms per macrocell
- Enhanced logic features:
  - 2-input Arithmetic Logic Unit in each macrocell
  - Dedicated fast carry network between macrocells
  - Wide AND capability in the Universal Interconnect Matrix
- Identical timing for all interconnect paths and for all macrocell logic paths
- 72 signal pins in the 84-pin packages
  - 42 I/Os, 12 inputs, 18 outputs
- Each input is programmable
  - Direct, latched, or registered
- I/O-pin is usable as input when macrocell is buried
- Two high-speed, low-skew global clock inputs
- Available in 68-pin and 84-pin PLCC/CLCC, 84-pin PGA packages

General Description

The XC7272A combines the classical features of the PAL-like CPLD architecture with innovative systems-oriented logic enhancements. This favors the implementation of fast state machines, large synchronous counters and fast arithmetic, as well as multi-level general-purpose logic. Performance, measured in achievable system clock rate and critical delays, is not only predictable, but independent of physical logic mapping, interconnect routing, and resource utilization. Performance, therefore, remains invariant between design iterations. The propagation delay through interconnect and logic is constant for any function implemented in any one of the output macrocells.

The functional versatility of the traditional programmable logic array architecture is enhanced through additional gating and control functions available in an Arithmetic Logic Unit (ALU) in each macrocell. Dedicated fast arithmetic carry lines running directly between adjacent macrocells and FBs support fast adders, subtractors and comparators of any length up to 72 bits.

This additional ALU in each macrocell can generate any combinatorial function of two sums of products, and it can generate and propagate arithmetic-carry signals between adjacent macrocells and Functional Blocks.

The Universal Interconnect Matrix (UIM) facilitates unrestricted, fixed-delay interconnects from all device inputs and macrocell outputs to any Function Block AND-array input. The UIM can also perform a logical AND across any number of its incoming signals on the way to any Functional Block, adding another level of logic without additional delay. This supports bidirectional loadable synchronous counters of any size up to 72 bits, operating at the specified maximum device frequency

As a result of these logic enhancements, the XC7272A can deliver high performance even in designs that combine large numbers of product terms per output, or need more layers of logic than AND-OR, or need a wide AND function in some of the product terms, or perform wide arithmetic functions.

Architectural Overview

Figure 1 shows the XC7272A structure. Eight Function Blocks(FBs) are all interconnected by a central UIM. Each FB receives 21 signals from the UIM and each FB produces nine signals back into the UIM. All device inputs are also routed via the UIM to all FBs. Each FB contains nine output macrocells that draw from a programmable AND array driven by the 21 signals from the UIM. Most Macro-cells drive a 3-state chip output. All feed back into the UIM.

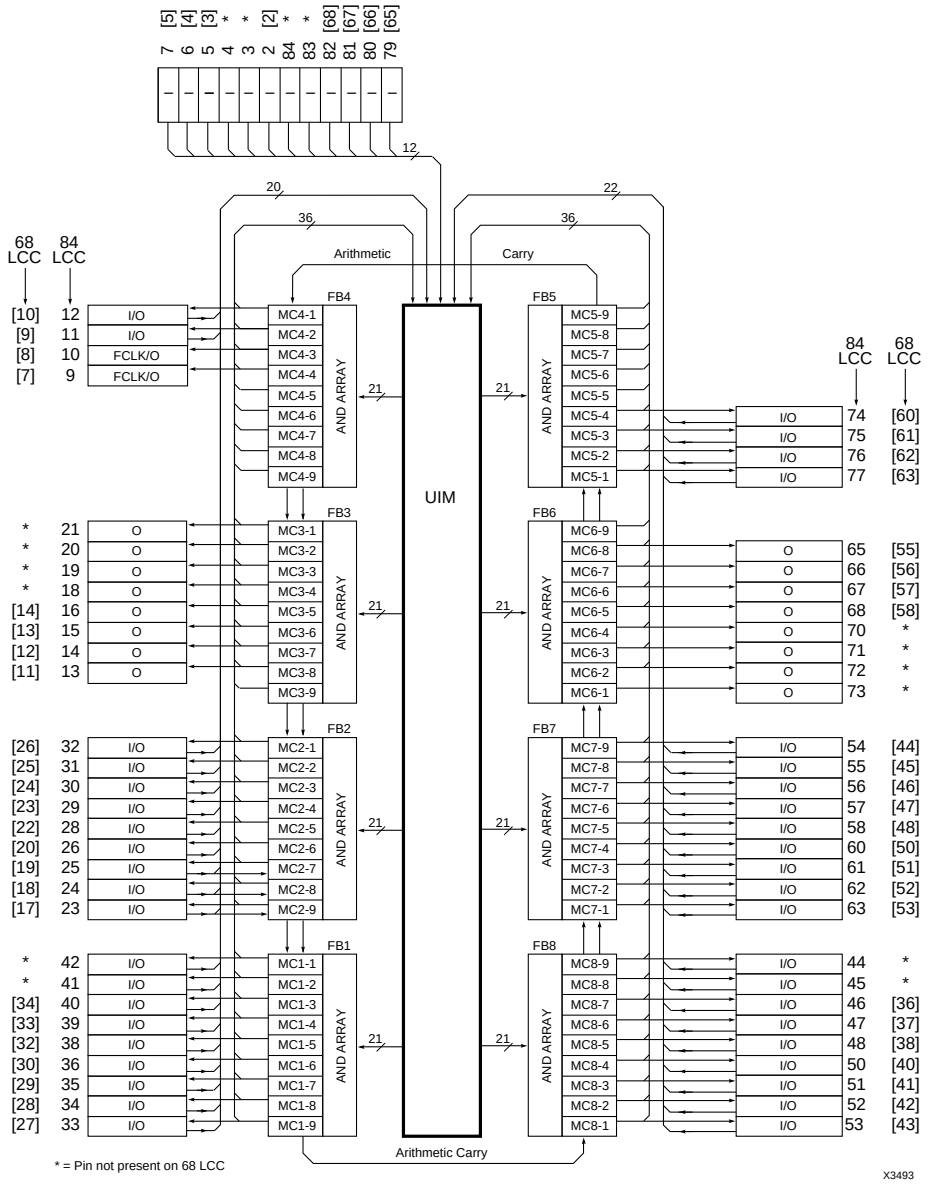


Figure 1: XC7272A Architecture

Function Blocks and Macrocells

The XC7272A contains 72 identical macrocells, grouped into eight FBs of nine macrocells each. Each macrocell is driven by product terms derived from the 21 inputs from the UIM into the Function Block. Figure 2 shows the macrocell structure.

Five product terms are private to each macrocell; an additional 12 product terms are shared among the nine macrocells in any Function Block. One private product term is a dedicated clock for the flip-flop in the macrocell.

The remaining four private product terms can be selectively ORed together with up to three of the shared product terms, to drive one input to an Arithmetic Logic Unit (ALU). The other input to the ALU is driven by the OR of up-to-nine product terms from the remaining shared product terms.

As a programmable option, two of the private product terms can be used for other purposes. One is the asynchronous active-High Reset of the macrocell flip-flop, the other can be either an asynchronous active-High Set of the macrocell flip-flop, or provide an active-High Output-Enable signal from any one of the Function Block inputs.

The ALU has two programmable modes. In the *logic mode,* it is a 2-input function generator, a 4-bit look-up table, that can be programmed to generate any Boolean function of its two inputs. It can OR them, widening the OR function to 16 inputs; it can AND them, which means that one sum of products can be used to mask the other; it can XOR them, toggling the flip-flop or comparing the two sums of products. Either or both of the sum-of-product inputs to the ALU can be inverted, and either or both can be ignored. The ALU can implement one additional layer of logic without any speed penalty.

In the *arithmetic mode,* the ALU block can be programmed to generate the arithmetic sum or difference of two operands, combined with a carry signal coming from the lower macrocell; it also feeds a carry output to the next higher macrocell. This carry propagation chain crosses the boundaries between FBs, but it can also be configured as a 0 or 1 when it enters a Function Block.

This dedicated carry chain overcomes the inherent speed and density problems of the traditional CPLD architecture, when trying to perform arithmetic functions like add, subtract, and magnitude compare.

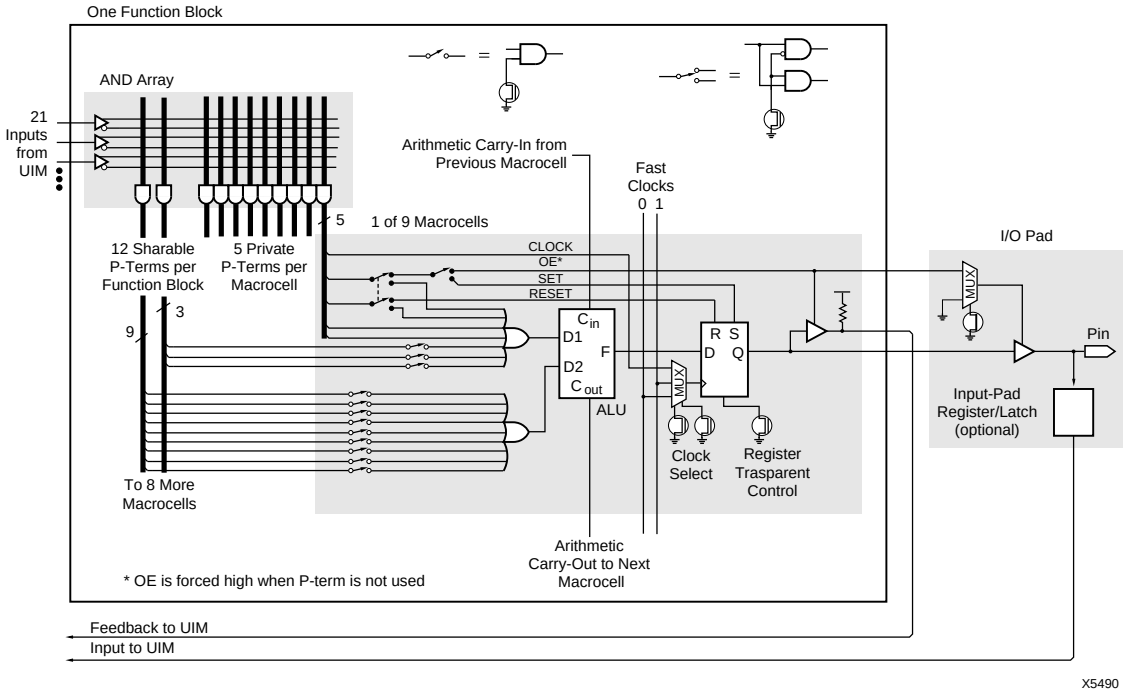


Figure 2: Function Block and Macrocell Schematic

The ALU output drives the D input of the macrocell flip-flop.

Each flip-flop has several programmable options:

One option is to eliminate the flip-flop by making it transparent, which makes the Q output identical with the D input, independent of the clock.

If this option is *not* programmed, the flip-flop operates in the conventional manner, triggered by the rising edge on its clock input.

The clock source is programmable: It is either the dedicated product term mentioned above, or it is one of the two global FastCLK signals that are distributed with short delay and minimal skew over the whole chip.

The asynchronous Set and Reset (Clear) inputs override the clocked operation. If both asynchronous inputs are active simultaneously, Reset overrides Set. Upon power-up, each macrocell flip-flop can be preloaded with either 0 or 1.

In addition to driving the chip output buffer, the macrocell output is also routed back as an input to the UIM. When the Output Enable product term mentioned above is not active, this feedback line is forced High and thus disabled.

Universal Interconnect Matrix

The UIM receives 126 inputs: 72 from the 72 macrocells, 42 from bidirectional I/O pins, and 12 from dedicated input pins. Acting as an unrestricted crossbar switch, the UIM generates 168 output signals, 21 to each Function Block.

Any one of the 126 inputs can be programmed to be connected to any number of the 168 outputs. The delay through the array is constant, independent of the apparent routing distance, the fan-out, fan-in, or routing complexity. Routability is not an issue: Any UIM input can drive any UIM output, even multiple outputs, and the delay is constant.

When multiple inputs are programmed to be connected to the same output, this output becomes the AND of the input signals if the levels are interpreted as active High. By choosing the appropriate signal inversion in the macrocell outputs and the Function Block AND-array input, this AND-logic can also be used to implement a NAND, OR, or NOR function, thus offering an additional level of logic without any speed penalty.

A macrocell feedback signal that is disabled by the output enable product term represents a High input to the UIM. Several such macrocell outputs programmed onto the same UIM output emulate a 3-state bus line. If one of the macrocell outputs is enabled, the UIM output assumes that same level.

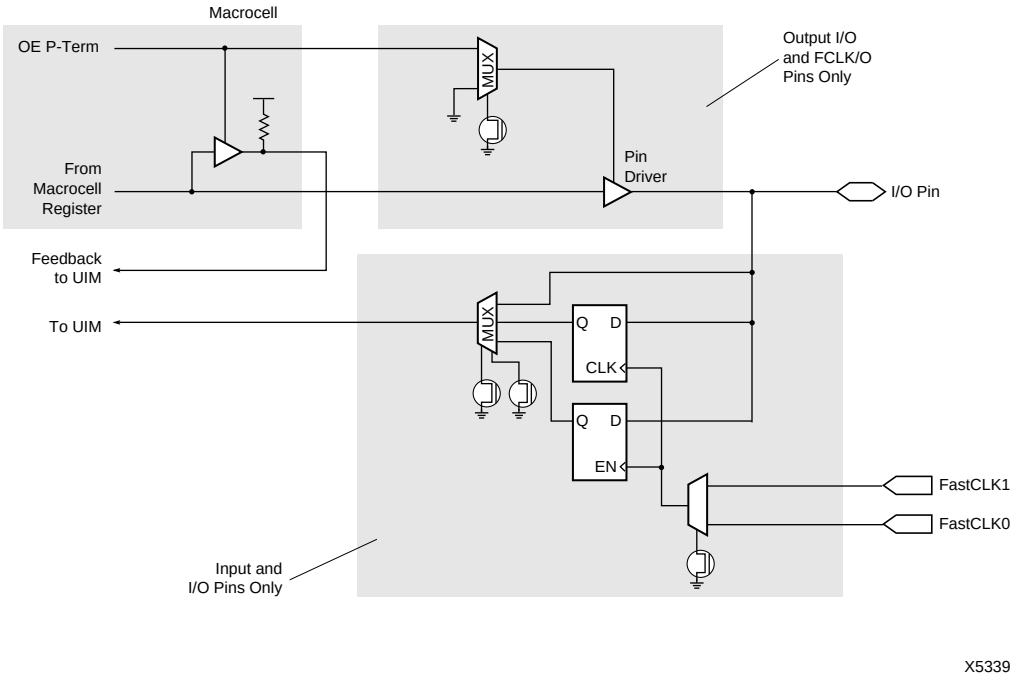


Figure 3: Input/Output Schematic

Outputs

Sixty of the 72 macrocells drive chip outputs directly through 3-state output buffers, each individually controlled by the Output Enable product term mentioned above. For bidirectional I/O pins, an additional programmable cell can optionally disable the output permanently. The buried flip-flop is then still available for internal feedback, and the pin can still be used as a separate input

Inputs

Each signal input to the chip is programmable as either direct, latched, or registered in a flip-flop. The latch and flip-flop can be programmed with either of the two FastCLK signals as latch enable or clock. The latch is transparent when FastCLK is High, and the flip-flop clocks on the rising edge of FastCLK. Registered inputs allow high system clock rates by pipelining the inputs before they incur the combinatorial delay in the device, in cases where a pipeline cycle is acceptable.

The direct, latched, or registered inputs then drive the UIM. There is no propagation-delay difference between pure inputs and I/O inputs.

Programming and Using the XC7272A

The features and capabilities described above are used by the Xilinx XACT*step* development software to program the device according to the specification given either through schematic entry, or through a behavioral description expressed in Boolean equations.

The user can specify a security bit that prevents any reading of the programming bit map after the device has been programmed and verified.

The device is programmed in a manner similar to an EPROM (ultra-violet light erasable read-only memory) using the Intel Hex or JEDEC format. Programming support is available from a number of programmer manufacturers. The UIM connections and Function Block AND-array connections are made directly by non-volatile EPROM cells. Other control bits are read out of the EPROM array and stored into latches just after power-up. This method, common among CPLD devices, requires either a very fast V_{CC} rise time (<5 µs) or the application of a master-reset signal delayed at least until V_{CC} has reached the required operating voltage. The latter can be achieved using a simple capacitor and pull-up resistor on the MR pin (the RC product should be larger than twice the V_{CC} rise time). The power-up or reset signal initiates a self-timed configuration period lasting about 350 µs (t_{RESET}), during which all device outputs remain disabled and programmed preload state values are loaded into the macrocell registers.

Unused input and I/O pins should be tied to ground or Vcc or some valid logic level. This is common practice for all CMOS devices to avoid dissipating excess current through the input-pad circuitry.

The recommended decoupling capacitance on the three V_{CC} pins should total 1 µF using high-speed (tantalum or ceramic) capacitors.

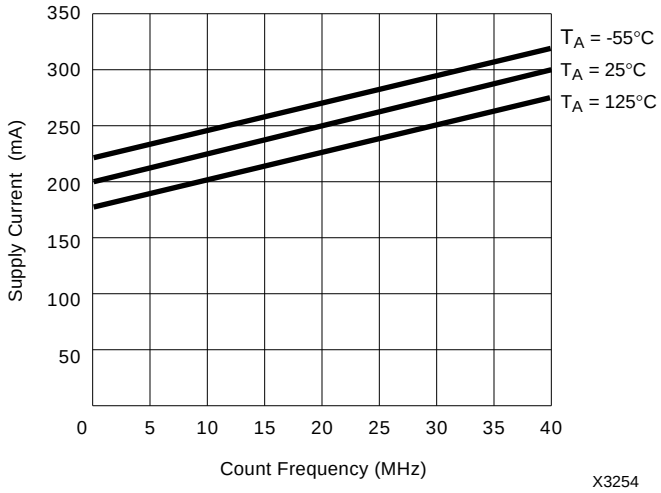


Figure 4: Typical I_{CC} vs. Frequency for XC7272A configured as sixteen 4-bit counters
(V_{CC} = +5.0 V, V_{IN} = V_{CC} or GND, all outputs open)

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{CC}	Supply voltage with respect to GND	-0.5 to V_{CC} +0.5	V
V_{IN}	DC Input voltage with respect to GND	-0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output with respect to GND	-0.5 to 7.0	V
T_{STG}	Storage temperature	-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10s @ 1/16 in. = 1.5 mm)	+260	°C

Warning: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CCINT}/ V_{CCIO}	Supply voltage relative to GND Commercial T_A = 0°C to 70°C	4.75	5.25	V
	Supply voltage relative to GND Industrial T_A = –40°C to 85°C	4.5	5.5	V
	Supply voltage relative to GND Military T_A = –55°C to T_C + 125°C	4.5	5.5	V
V_{IH}	High-level input voltage	2.0	V_{CC} +0.5	V
V_{IL}	Low-level input voltage	0	0.8	V

DC Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{OH}	TTL High-level output voltage	I_{OH} = -4.0 mA V_{CC} = Min	2.4		V
V_{OL}	TTL Low-level output voltage	I_{OL} = 8 mA V_{CC} = Min		0.5	V
I_{CC}	Supply current	V_{IN} = 0 V V_{CC} = Max f = 0 MHz	222 Typ		mA
I_{IL}	Input leakage current		-10	+10	µA
I_{OZ}	Output high-Z leakage current		-100	+100	µA
C_{IN}	Input capacitance (sample tested)			10	pF

AC Timing Requirements

Symbol	Parameter	Fig.	XC7272A-25		XC7272A-20		XC7272A-16 (Com/Ind only)		Units
			Min	Max	Min	Max	Min	Max	
f_{CYC} (Note 1)	Max sequential toggle frequency (with feedback) using FastCLK		40		50		55		MHz
f_{CYC1} (Note 1)	Max sequential toggle frequency (with feedback) using a Product-Term Clock		40		50		55		MHz
f_{CLK} (Note 2)	Max macrocell register transmission frequency (without feedback) using FastCLK		40		50		55		MHz
f_{CLK1} (Note 2)	Max macrocell register transmission frequency (without feedback) using a Product-Term Clock		40		50		55		MHz
f_{CLK2} (Note 2)	Max input register transmission frequency (without feedback) using FastCLK		67		67		67		MHz
f_{CLK3} (Note 1)	Max input register to macrocell register pipeline frequency using FastCLK	7	40		50		60		MHz
t_{WL}	FastCLK Low pulse width	11	7.5		7.5		6		ns
t_{WH}	FastCLK High pulse width	11	7.5		7.5		6		ns
f_{TOG}	Export Control Max. flip-flop toggle rate			67		67		83	MHz
t_{W1}	Product-term clock pulse width (active/inactive)	11	10		9		7		ns
t_{SU}	Input to macrocell register set-up time before FastCLK	9	24		19		15		ns
t_{H}	Input to macrocell register hold time after FastCLK	9	-7		-4		-4		ns
t_{SU1} (Note 1)	Input to macrocell register set-up time before Product-term clock	8	10		8		6		ns
t_{H1}	Input to macrocell register hold time after Product-term clock	8	0		0		0		ns
t_{SU2}	Input to register/latch set-up time before FastLCK	10	8		8		6		ns
t_{H2}	Input to register/latch hold time after FastLCK	10	0		0		0		ns
t_{WA}	Set/Reset pulse width	11	12		10		8		ns
t_{RA}	Set/Reset input recovery set-up time before FastCLK	11	20		20		16		ns
t_{HA}	Set/Reset input hold time after FastCLK	11	-5		-3		-3		ns
t_{RA1}	Set/Reset input recovery set-up time before Product-term clock	11	6		5		4		ns
t_{HA1}	Set/Reset input hold time after Product-term clock	11	9		8		6		ns
t_{HRS}	Set/Reset input hold time after Reset/Set inactive		10		8		6		ns

Notes: 1. Specifications account for logic paths that use the maximum number of available product terms and the ALU.
2. Not tested but derived from appropriate pulse-widths, set-up time and hold-time measurements.

Propagation Delays

Symbol	Parameter	Fig.	XC7272A-25		XC7272A-20		XC7272A-16 (Com/Ind only)		Units
			Min	Max	Min	Max	Min	Max	
t_{CO}	FastCLK input to registered output delay	11	5	16	3	14	3	12	ns
t_{CO1}	P-term clock input to registered output delay	11	10	30	6	25	6	21	ns
t_{AO}	Set/Reset input to registered output delay	11	13	40	8	32	8	25	ns
t_{PDD} (Note 1)	Input to non-registered output delay	11	13	40	8	32	8	25	ns
t_{OE}	Input to output enable	11	11	32	7	25	7	22	ns
t_{OD}	Input to output disable		11	32	7	25	7	22	ns

Note: 1. Specifications account for logic paths which use the maximum number of available product terms and the ALU.

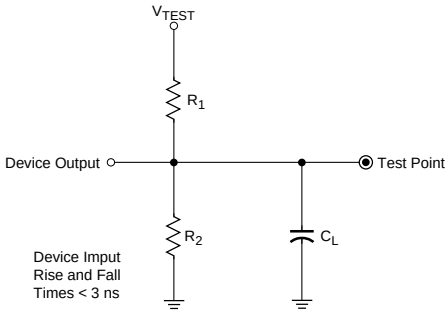
Incremental Parameters

Symbol	Parameter	Fig.	XC7272A-25		XC7272A-20		XC7272A-16 (Com/Ind only)		Units
			Min	Max	Min	Max	Min	Max	
t_{PDT1} (Note 2)	Arithmetic carry delay between adjacent macrocells	12		1.6		1.2		1	ns
t_{PDT8} (Note 2)	Arithmetic carry delay through 9 adjacent macrocells in a FB	12		10		8		6	ns
t_{PDT9} (Note 2)	Arithmetic carry delay through 10 macrocells from macrocell #n to macrocell #n in next FB	12		14		12		10	ns
t_{COF}	Incremental delay from FastCLK net to registered output feedback	13		1		1		1	ns
t_{COF1}	Incremental delay from UIM-input (for P-term clock) to registered macrocell feedback	13		1.5		12		10	ns
t_{COF2} (Note 3)	Incremental delay from FastCLK net to latched/registered UIM-input	13		1		1		1	ns
t_{PDF} (Note 1)	Incremental delay from UIM-input to non-registered macrocell feedback	13		25		19		14	ns
t_{AOF}	Incremental delay from UIM-input (Set/Reset) to registered macrocell feedback	13		25		19		14	ns
t_{OEF} t_{ODF}	Incremental delay from UIM-input (used as output-enable/disable) to macrocell feedback	13		17		12		11	ns
$t_{IN} + t_{OUT}$ (Note 4)	Propagation delay through unregistered input pad (to UIM) plus output pad driver (from macrocell)	13		15		13		11	ns

Notes: 1. Specifications account for logic paths that use the maximum number of available product terms and the ALU.
2. Arithmetic carry delays are measured as the increase in required set-up time to adjacent macrocell(s) for an adder with registered outputs.
3. Parameter t_{COF2} is derived as the difference between the clock period for pipelining input-to-macrocell registers ($1/f_{CLK3}$) and the non-registered input set-up time (t_{SU}).
4. Parameter t_{IN} represents the delay from an input or I/O pin to a UIM-input (or from a FastCLK pin to the Fast CLK net); t_{OUT} represents the delay from a macrocell output (feedback point) to an output or I/O pin. Only the sum of $t_{IN} + t_{OUT}$ can be derived from measurements, e.g., $t_{IN} + t_{OUT} = t_{SU} + t_{CO} - 1/f_{CYC}$.

Power-up/Reset Timing Parameters

Symbol	Parameter	Min	Typ	Max	Units
t_{WMR}	Master Reset input Low pulse width	100			ns
t_{rVCC}	V_{CC} rise time (if MR not used for power-up)			5	µs
t_{RESET}	Configuration completion time (to outputs operational)		350	1000	µs



Output Type	V_{CCIO}	V_{TEST}	R_1	R_2	C_L
O	5.0 V	5.0 V	450 Ω	245 Ω	35 pF

X3490

Figure 5: AC Load Circuit

Timing and Delay Path Specifications

The delay path consists of three blocks that can be connected in series:

- Input Buffer and associated latch or register
- Logic Resource (UIM, AND-array and macrocell)
- Three-state Output Buffer

All inputs have the same delay, regardless of fan-out or location. All logic resources have the same delay, regardless of logic complexity, interconnect topology or location on the chip. All outputs have the same delay. The achievable clock rate is, therefore, determined only by the input method (direct, latched or registered) and the number of times a signal passes through the combinatorial logic.

Timing and Delay Path Descriptions

Figure 6 defines the maximum clock frequency (with feedback). Any macrocell output can be fed back to the UIM as an input for the next clock cycle. Figure 6 shows the relevant delay path. The parameters f_{CYC} and f_{CYC1} specify the maximum operating frequency for FastCLK and product-term clock operation respectively.

Figure 7 specifies the max operating frequency (f_{CLK3}) for pipelined operation between the input registers and the macrocell registers, using FastCLK.

Figure 8 defines the set-up and hold times from the data inputs to the product-term clock used by the output register.

Figure 9 defines the set-up and hold times from the data inputs to the FastCLK used by the output register.

Figure 10 defines the set-up and hold times from the data input to the FastCLK used in an input register.

Figure 11 shows the waveforms for the macrocell and control paths

Figure 12 defines the carry propagation delays between macrocells and between FBs. The parameters describe the delay from the C_{IN}, D1 and D2 inputs of a macrocell ALU to the C_{IN} input of the adjacent macrocell ALU. These delays must be added to the standard macrocell delay path (t_{PD} or t_{SU}) to determine the performance of an arithmetic function.

Figure 13 defines the incremental parameters for the standard macrocell logic paths. These incremental parameters are used in conjunction with pin-to-pin parameters when calculating compound logic path timing. Incremental parameters are derived indirectly from other pin-to-pin measurement.

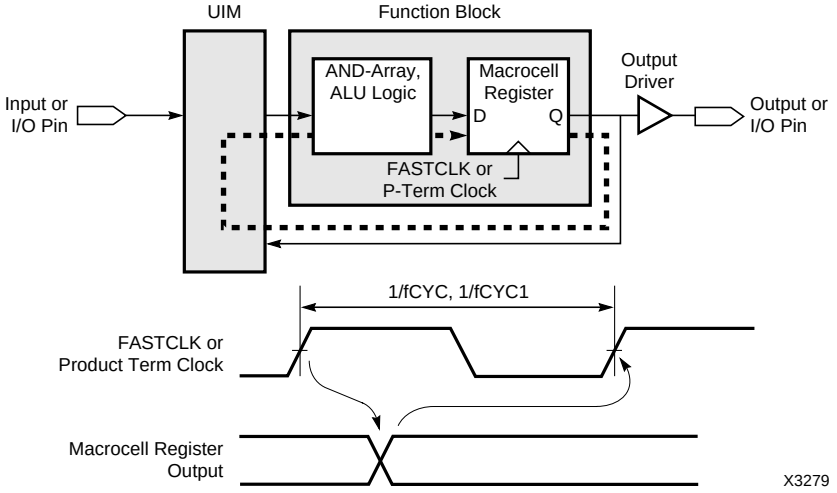


Figure 6: Delay Path Specification for f_{CYC} and f_{CYC1}

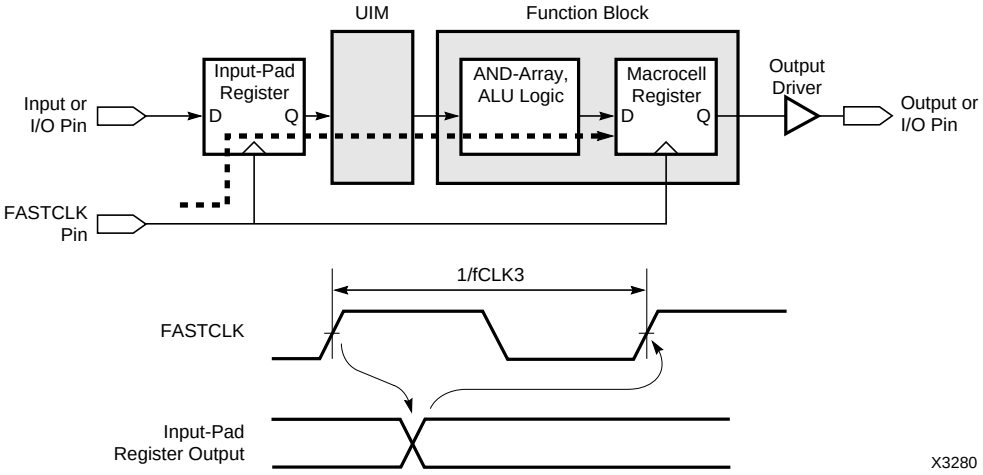


Figure 7: Delay Path Specification for f_{CLK3}

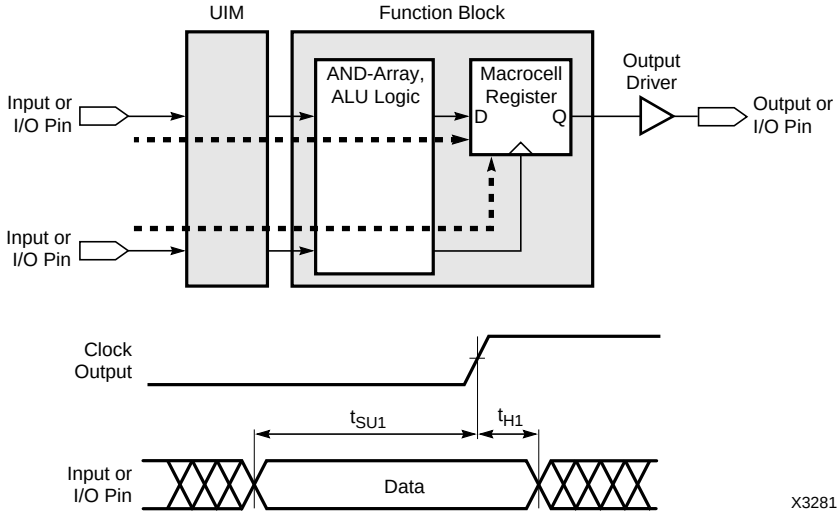


Figure 8: Delay Path Specification for f_{SU1} and f_{H1}

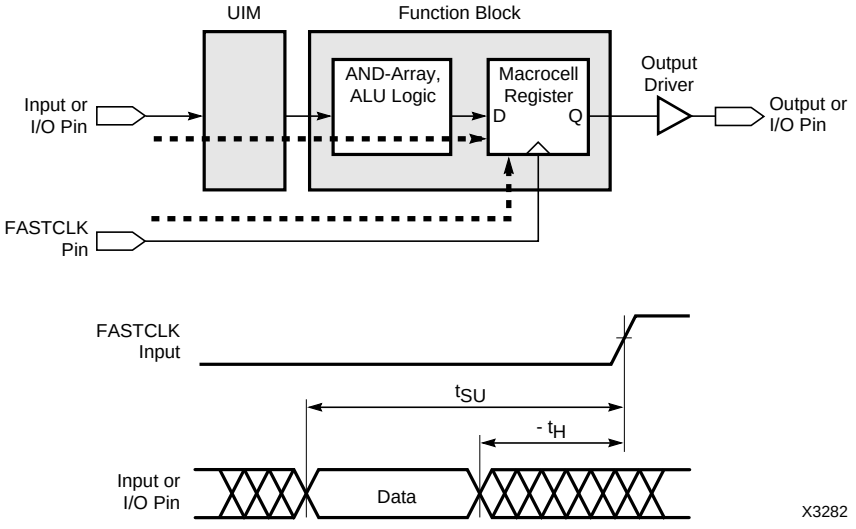


Figure 9: Delay Path Specification for f_{SU} and f_H

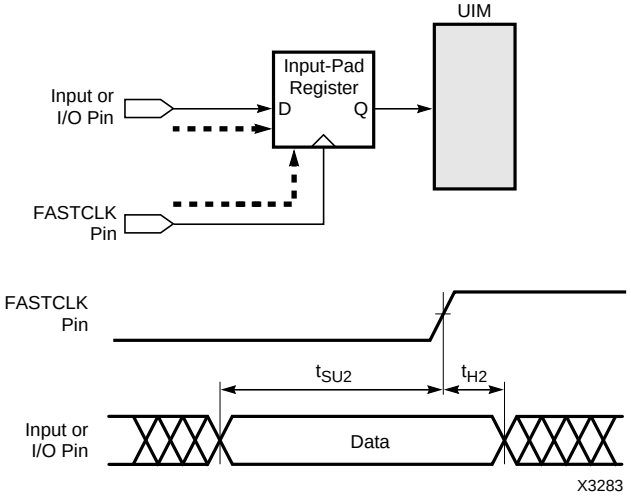


Figure 10: Delay Path Specification for f_{SU2} and f_{H2}

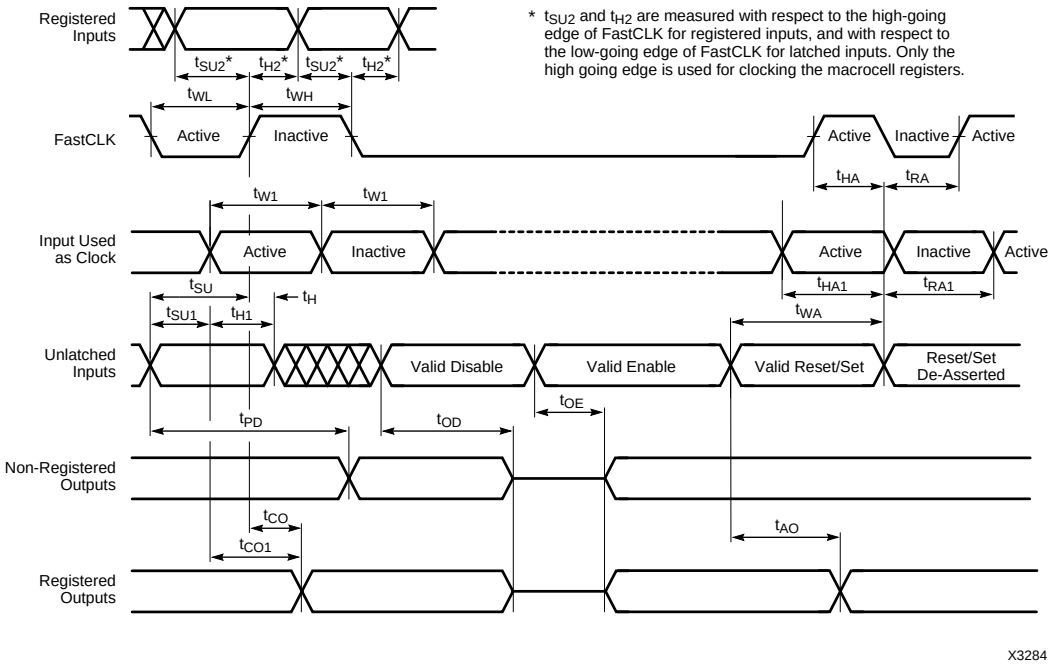


Figure 11: Principal Pin-to-Pin Measurements

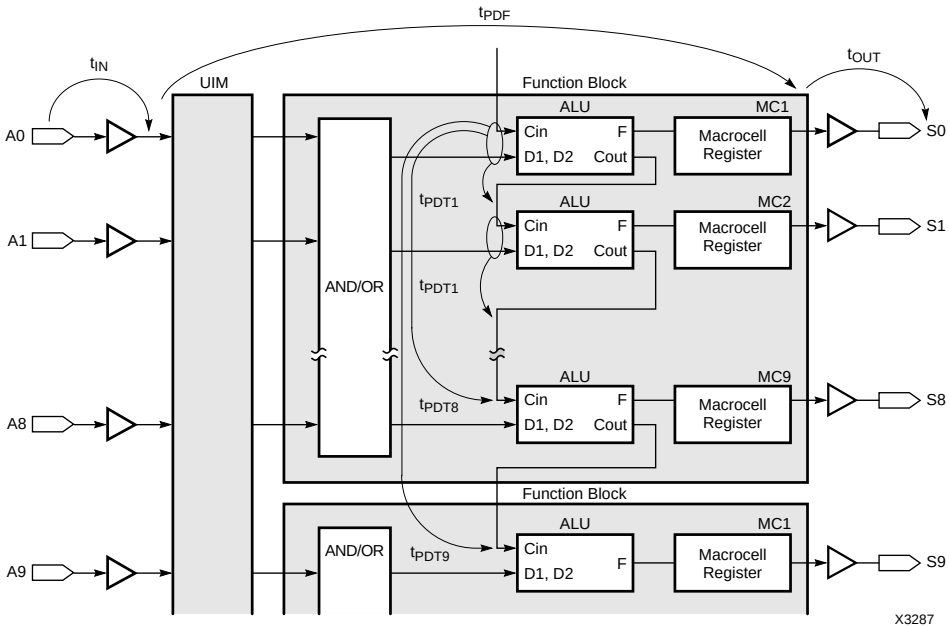


Figure 12: Arithmetic Timing Parameters

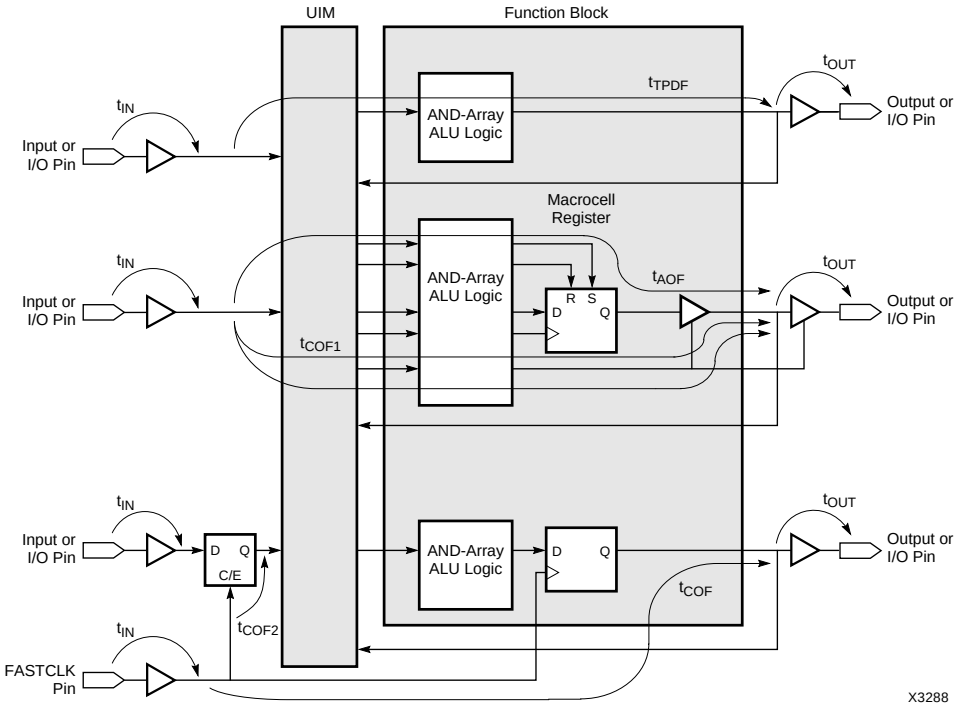


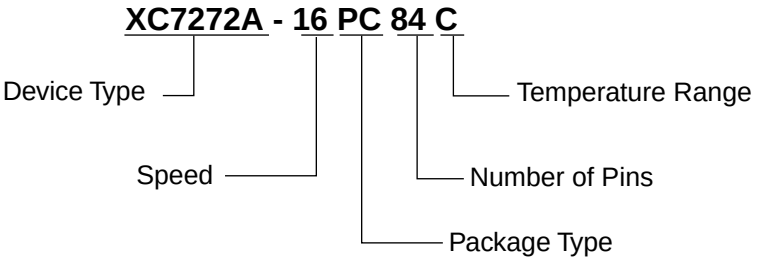
Figure 13: Incremental Timing Parameters

XC7372 Pinouts

PC68	in	XC7272A	out	PC84	PG84
1	Master Reset			1	F-9
2	Input			2	F-11
-	Input			3	E-11
-	Input			4	E-10
3	Input			5	E-9
4	Input			6	D-11
5	Input			7	D-10
6		**GND**		8	C-11
7	Fast CLK0		MC4-4	9	B-11
8	Fast CLK1		MC4-3	10	C-10
9	Input		MC4-2	11	A-11
10	Input		MC4-1	12	B-10
11			MC3-8	13	B-9
12			MC3-7	14	A-10
13			MC3-6	15	A-9
14			MC3-5	16	B-8
15		**GND**		17	A-8
-			MC3-4	18	B-6
-			MC3-3	19	B-7
-			MC3-2	20	A-7
-			MC3-1	21	C-7
16		**Vcc**		22	C-6
17	Input		MC2-9	23	A-6
18	Input		MC2-8	24	A-5
19	Input		MC2-7	25	B-5
20	Input		MC2-6	26	C-5
21		**GND**		27	A-4
22	Input		MC2-5	28	B-4
23	Input		MC2-4	29	A-3
24	Input		MC2-3	30	A-2
25	Input		MC2-2	31	B-3
26	Input		MC2-1	32	A-1
27	Input		MC1-9	33	B-2
28	Input		MC1-8	34	C-2
29	Input		MC1-7	35	B-1
30	Input		MC1-6	36	C-1
31		**GND**		37	D-2
32	Input		MC1-5	38	D-1
33	Input		MC1-4	39	E-3
34	Input		MC1-3	40	E-2
-	Input		MC1-2	41	E-1
-	Input		MC1-1	42	F-2

PC68	in	XC7272A	out	PC84	PG84
35		**Vcc**		43	F-3
-	Input		MC8-9	44	G-3
-	Input		MC8-8	45	G-1
36	Input		MC8-7	46	G-2
37	Input		MC8-6	47	F-1
38	Input		MC8-5	48	H-1
39		**GND**		49	H-2
40	Input		MC8-4	50	J-1
41	Input		MC8-3	51	K-1
42	Input		MC8-2	52	J-2
43	Input		MC8-1	53	L-1
44	Input		MC7-9	54	K-2
45	Input		MC7-8	55	K-3
46	Input		MC7-7	56	L-2
47	Input		MC7-6	57	L-3
48	Input		MC7-5	58	K-4
49		**GND**		59	L-4
50	Input		MC7-4	60	J-5
51	Input		MC7-3	61	K-5
52	Input		MC7-2	62	L-5
53	Input		MC7-1	63	K-6
54		**Vcc**		64	J-6
55			MC6-8	65	J-7
56			MC6-7	66	L-7
57			MC6-6	67	K-7
58			MC6-5	68	L-6
59		**GND**		69	L-8
-			MC6-4	70	K-8
-			MC6-3	71	L-9
-			MC6-2	72	L-10
-			MC6-1	73	K-9
60	Input		MC5-4	74	L-11
61	Input		MC5-3	75	K-10
62	Input		MC5-2	76	J-10
63	Input		MC5-1	77	K-11
64		**GND**		78	J-11
65	Input			79	H-10
66	Input			80	H-11
67	Input			81	F-10
68	Input			82	G-10
-	Input			83	G-11
-	Input			84	G-9

Ordering Information



Speed Options

-25	25 ns (40 MHz) sequential cycle time
-20	20 ns (50 MHz) sequential cycle time
-16	16 ns (60 MHz) sequential cycle time (commercial/industrial only)

Packaging Options

PC68	68-Pin Plastic Leaded Chip Carrier
WC68	68-Pin Windowed Ceramic Leaded Chip Carrier
PC84	84-Pin Plastic Leaded Chip Carrier
WC84	84-Pin Windowed Ceramic Leaded Chip Carrier
PG84	84-Pin Ceramic Windowed Pin Grid Array

Temperature Options

C	Commercial	0°C to 70°C
I	Industrial	-40°C to 85°C
M	Military	-55°C (Ambient) to 125°C (Case)

Component Availability

Pins		**68**		**84**		
Type		**Plastic PLCC**	**Ceramic CLCC**	**Plastic PLCC**	**Ceramic CLCC**	**Ceramic PGA**
Code		**PC68**	**WC68**	**PC84**	**WC84**	**PG84**
XC7272A	–25	CI	CI	CI	CIM	CI
	–20	CI	CI	CI	CIM	CI
	–16	CI	CI	CI	CI	CI

C = Commercial = 0° to +70°C I = Industrial = –40° to 85°C M = Military = –55°C(A) to 125°C (C)